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Exercise for the lecture
Embedded Systems
Wintersemester 17/18

Written Exercise Sheet 4

Hints: These assignments will be discussed at E23 from 10:15 AM - 11:45 AM on 19. Dez. 2017. You are not obligated to turn in the solutions.

1 FPGA

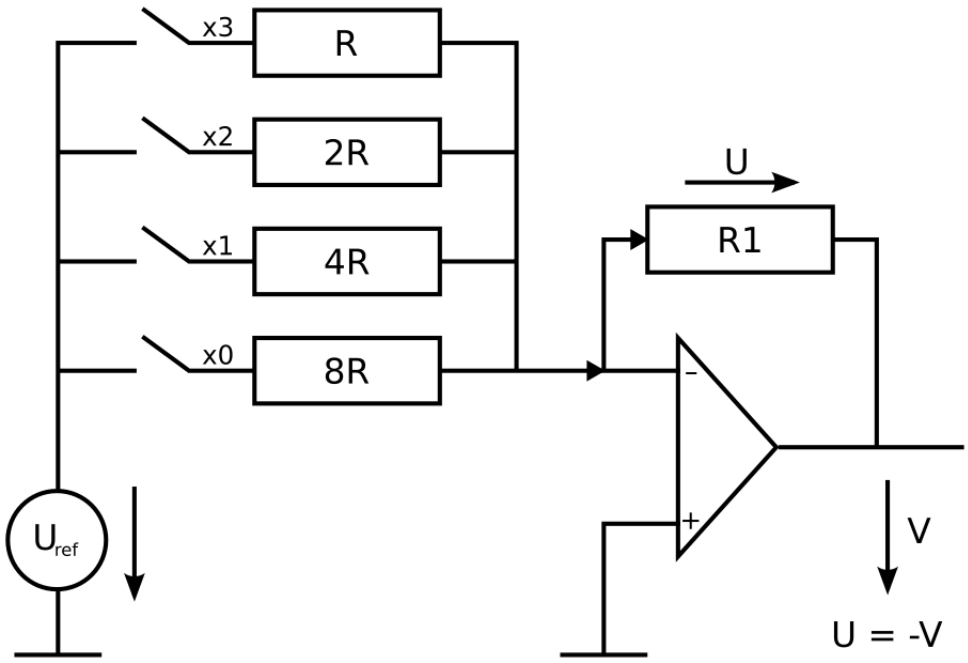
Many FPGAs use look-up tables for Boolean functions. Earlier FPGAs used look-up tables for 4 variables (memories with 4 address inputs). Configurations could be used to implement any Boolean function of 4 variables. How many Boolean functions of 4 variables exist? We ignore symmetries and also count simple functions like constant functions.

2 Memory Hierarchy

What is the *memory wall* problem? How do scratchpad memory (SPM) and Cache memory work? What are the corresponding advantages of SPM and Cache, respectively?

3 D/A-Converter

Consider the following D/A converter:



Assume $U_{ref} = 5V,\ R = 1k\Omega$ to be given.

- How must the feedback resistor R_1 be chosen if the digital values shall be mapped to a voltage range from $0V - 10V$?

- The accuracy of the D/A conversion by means of a summation current transformer strongly depends on the accuracy (tolerance) of the chosen resistors. If the deviation from the set value is too large, the delivered current for a certain binary value b may be less than that for the next lower binary value $b-1$ (monotonicity error).
  - With respect to which binary value may a monotonicity error probably have the largest impact?
  - Calculate the current flow for both values.
  - By which maximum value of Ω may resistor R deviate upwards such that no monotonicity error occurs?

Which of the resistors at the input have the greatest impact on the converter's accuracy? Which is the maximum tolerance this resistor may have with respect to the converter resolution?

4 RTOS

- What are the requirements of an RTOS?
- Explain how an RTOS schedules real-time tasks under fixed-priority scheduling.
- Explain how to extend the standard OSes to have real-time extensions. In such cases, explain whether real-time tasks can use all the system calls in the standard OSes or not.

5 Interrupt Handling

RTOSes require to have a bounded delay for handling interrupts. If an interrupt is detected, the processor performs a context switch (temporarily pauses the execution of the current tasks and executes a designated interrupt service routine (ISR)). This may increase the response time. Explain how interrupts should be handled in RTOSes to reduce the influence on the real-time tasks in the system.

Hint: You can refer to Sec. 2 in the following article: Björn B. Brandenburg, Hennadiy Leontyev, James H. Anderson: An overview of interrupt accounting techniques for multiprocessor real-time systems. Journal of Systems Architecture - 57(6): 638-654 (2011)

6 Aperiodic Scheduling

Consider a system with three tasks, all arriving at $t = 0$:

- Task T1 has an execution time of 9 time units and an (absolute) deadline at time 25.
- Task T2 has an execution time of 3 time units and an (absolute) deadline at time 10.
- Task T3 has an execution time o 10 time units and an (absolute) deadline at time 15.

Which algorithm would you use to schedule the three tasks and why?

7 Schedulability Tests

For the previous example, provide

- one necessary test,
- one exact test
- and one sufficient test

for schedulability!

8 EDF Scheduling

Consider a system with three tasks:

- Task T1 arrives at time 0, has an execution time of 9 time units and a deadline at time 35.
- Task T2 arrives at time 5, has an execution time of 3 time units and a deadline at time 27.
- Task T3 arrives at time 6, has an execution time o 10 time units and a deadline at time 29.

Generate a schedule for this task system using the earliest deadline first (EDF) scheduling policy!

9 Least Laxity Scheduling

Generate a schedule for the previous task system using the least laxity scheduling policy!