

Title: The Design of the PRIPS Microprocessor

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Abstract:

The PRIPS microprocessor was recently designed at the University of Dortmund, Lehrstuhl Informatik XII. PRIPS is a coprocessor with an RISC-like instruction set. The supported data types and some of the instructions are oriented towards supporting the execution of PROLOG programs. The design was performed by a project group consisting of 10 students. Such project groups are one of the key features of the computer science curriculum at Dortmund. The project group was partitioned into three subgroups. The first subgroup was responsible for everything related to compiling PROLOG programs into machine code. This group designed the instruction set of PRIPS. The first approach was to consider implementing the Warren abstract machine (WAM). This approach was rejected because of the size of the required microcode. Therefore, it was decided, to implement a RISC-like instruction set with some special instructions for PROLOG. With this approach, PROLOG-programs are first compiled into WAM-code. WAM instructions are then expanded into RISC instructions. The first subgroup also analysed the effect of different options for caches on the performance.

The second subgroup designed the register-transfer structure for the given instruction set. To this end, semantics of the instruction set was described in the hardware description language MIMOLA. Using the TODOS high-level synthesis system designed at the Universities of Kiel and Dortmund, an initial RT-structure was generated. Subsequent improvements were added by using the retargetable code generator MSSQ (see paper by Marwedel at EDAC-EUROASIC-93 for a description of the design process). The final register transfer structure contains a register file of 32 registers of 32 bits and an ALU with very sophisticated concurrent tag checking modes. In order to achieve maximum flexibility, it was decided to implement an on-chip loadable microstore. In order to improve testability of the chip, PRIPS uses external clock generation and a scan-path design for the controller.

The third group entered the PRIPS design into a commercial Cadence EDGE CAD database. Due to the problems with the EDIF interface, the design was entered using schematics entry. Final layout was also obtained with EDGE. Several iterations were required to meet design constraints. The final chip size is 12 by 8 mm for the ES2 1.5 μ m CMOS process.

PRIPS has been submitted to EUROCHIP for fabrication. After some delay, caused by undocumented features of format converters, 30 samples were received in February, 1993. The setup used for testing basically consists of an Hewlett Packard 16500A tester, which is linked to a Sun workstation and programmed using the TSSI software package. First results indicate that some of the chips are working. However, detailed results are not available yet.