

---

## Contents

<b>Acknowledgements .....</b>	<b>xi</b>
<b>1 Abstract .....</b>	<b>1</b>
<b>2 Introduction .....</b>	<b>3</b>
2.1 Motivation .....	5
2.2 Contributions of this Work .....	11
2.3 Overview .....	13
<b>3 Models and Tools.....</b>	<b>15</b>
3.1 Instruction Set Architecture Model .....	17
3.2 Memory Models .....	18
3.2.1 SRAM .....	19
3.2.2 DRAM.....	21
3.2.3 Flash Memory .....	24
3.2.4 Caches .....	25
3.3 Timing Models.....	29
3.3.1 Processor and Instruction Timing .....	29
3.3.2 Memory Timing.....	31
3.4 Energy Models .....	36
3.4.1 Sources of Energy Dissipation .....	37
3.4.2 Processor Energy .....	40
3.4.3 Memory Energy .....	45
3.5 Simulation Models .....	61
3.5.1 Processor Simulation Model .....	61
3.5.2 Memory Simulation Model.....	66
3.6 The encc Compiler Framework .....	75
3.6.1 Workflow .....	77
3.6.2 enprofiler .....	81
3.6.3 Memory Architecture Aware Compilation .....	82

<b>4    Scratchpad Memory Optimizations .....</b>	89
4.1    Related Work .....	90
4.2    Multi Memory Optimization .....	97
4.2.1    Memory Objects .....	99
4.2.2    Prerequisites .....	100
4.2.3    Energy Functions .....	101
4.2.4    The Base model .....	102
4.2.5    The Top-Down Model .....	104
4.2.6    The Bottom-Up Model .....	111
4.2.7    The ARM TCM Model .....	115
4.2.8    Leakage-Energy Aware Memory Configuration .....	117
4.2.9    Results for Multi Memory Optimization .....	120
4.3    Impact of Scratchpad Allocation Techniques on WCET .....	136
4.3.1    Related Work .....	140
4.3.2    Tools and Workflow .....	142
4.3.3    Required Annotation Information .....	145
4.3.4    Benchmarks and Memory Hierarchy Configuration .....	151
4.3.5    WCET Results for Static Allocation .....	152
4.3.6    WCET Results for Dynamic Allocation .....	161
<b>5    Main Memory Optimizations .....</b>	171
5.1    Related Work .....	172
5.2    Main Memory Power Management .....	174
5.2.1    Motivating Example .....	177
5.2.2    Prerequisites .....	178
5.2.3    Memory Objects and Energy Functions .....	179
5.2.4    Binary Decision Variables .....	182
5.2.5    Objective Function .....	184
5.2.6    Constraints .....	184
5.2.7    Results for Main Memory Power Management .....	186
5.3    Execute-In-Place using Flash Memories .....	192
5.3.1    Analysis of the Copy Function .....	194
5.3.2    Main Memory Partitioning .....	195
5.3.3    Prerequisites .....	197
5.3.4    Preselection of Memory Objects to enable Deep Power Down .....	199
5.3.5    Formalization of the Preselection Algorithm .....	203
5.3.6    Formalization of the XIP Allocation Problem .....	204
5.3.7    Results for XIP .....	207
<b>6    Register File Optimization .....</b>	217
6.1    Related Work .....	218
6.2    Implementation of the Register File .....	219
6.3    Register Allocation and Lifetime Analysis .....	220
6.4    Workflow and Methodology .....	222

6.5	Benchmark Suite .....	224
6.5.1	Results for the Ratio of Spill Code to Total Code Size..	224
6.5.2	Results for the Number of Cycles .....	226
6.5.3	Results for Energy Consumption .....	229
6.6	Compiler Guided Choice of Register File Size .....	230
<b>7</b>	<b>Summary</b> .....	<b>233</b>
<b>8</b>	<b>Future Work</b> .....	<b>239</b>
<b>References</b> .....		<b>243</b>
<b>Index</b> .....		<b>255</b>