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Embedded System Hardware
- Reconfigurable Hardware -

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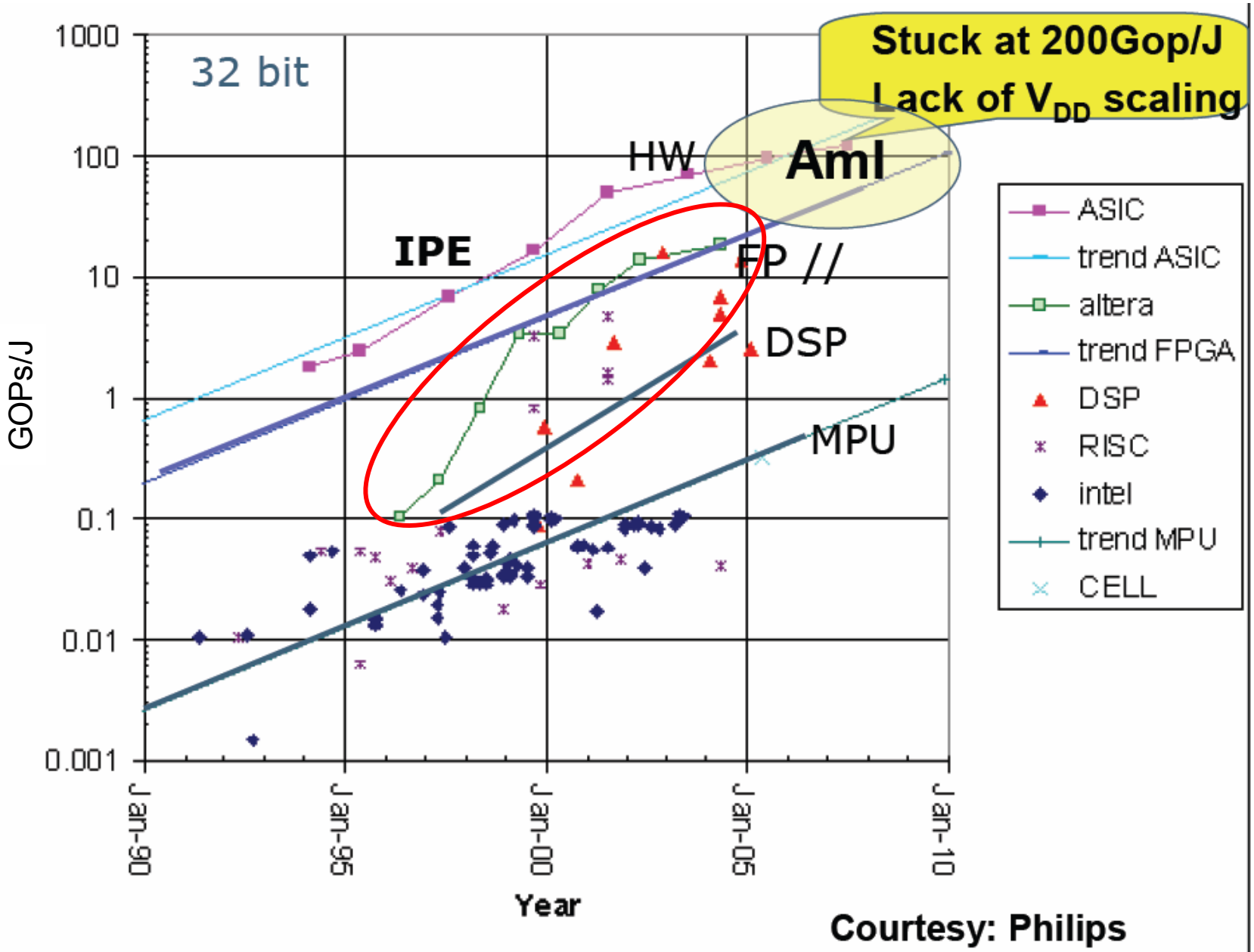
2008/11/15

Energy Efficiency of FPGAs



Courtesy: Philips
© Hugo De Man, IMEC, 2007

Reconfigurable Logic

Full custom chips may be too expensive, software too slow.

Combine the speed of HW with the flexibility of SW

- ☞HW with programmable functions and interconnect.
- ☞Use of configurable hardware;
  common form: field programmable gate arrays (FPGAs)

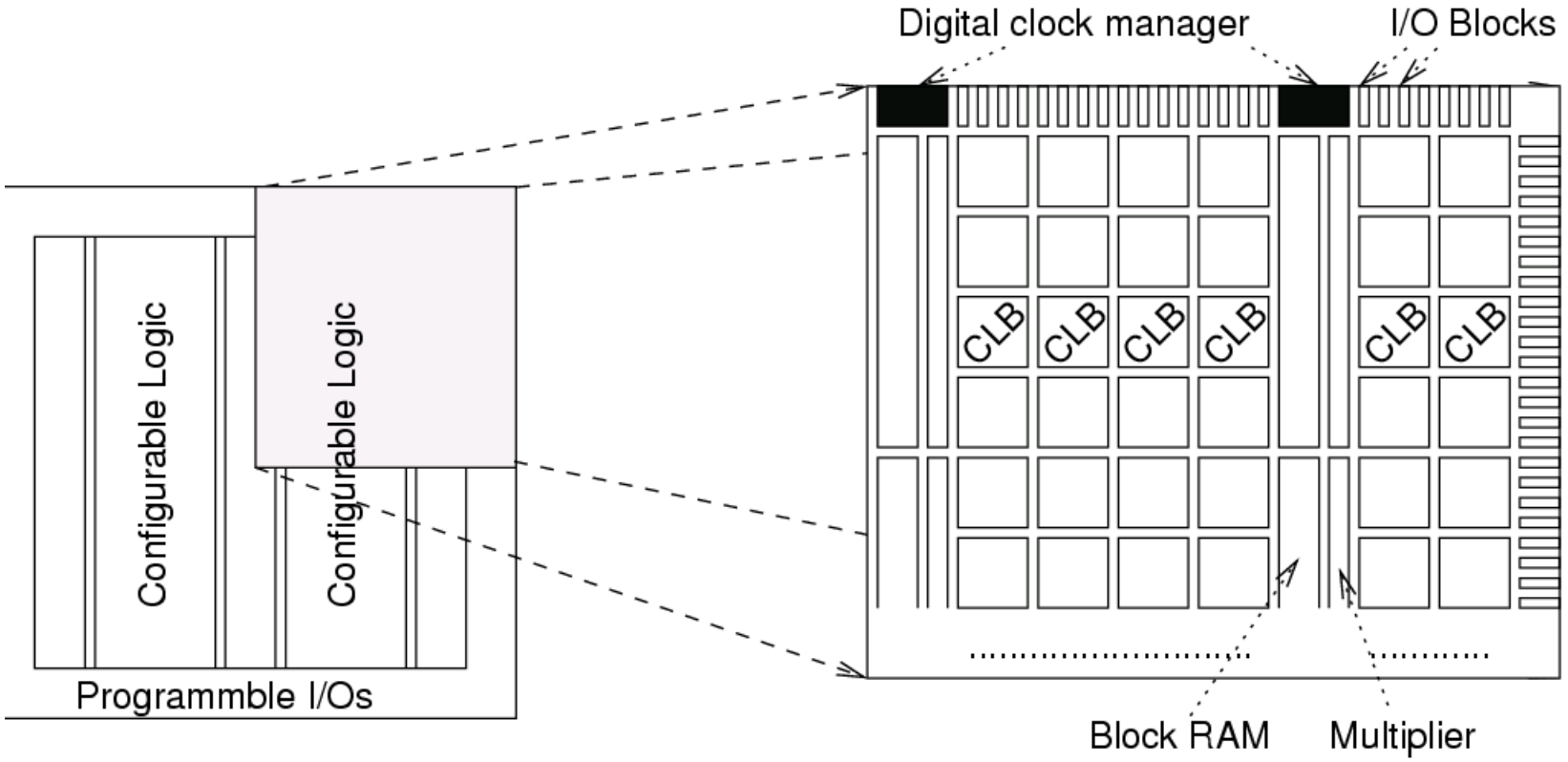
Applications: bit-oriented algorithms like

- encryption,
- fast “object recognition“ (medical and military)
- Adapting mobile phones to different standards.

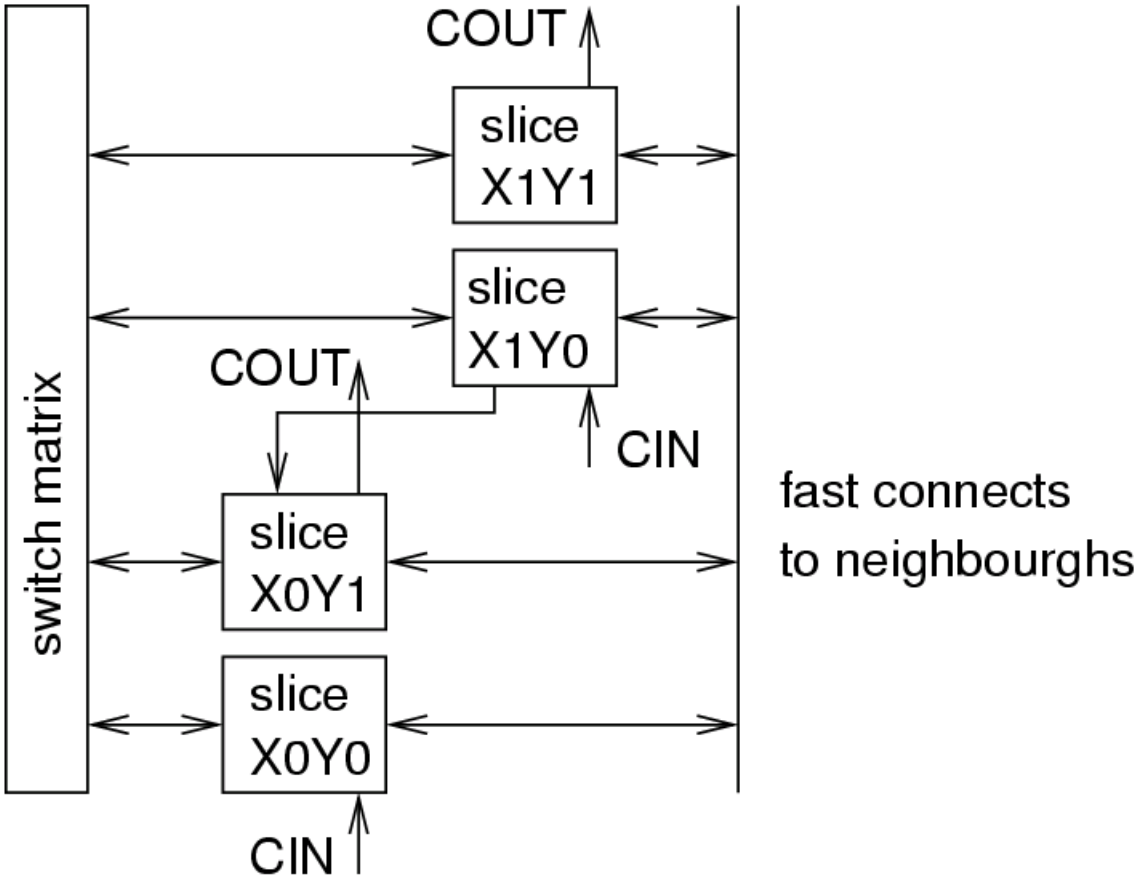
Very popular devices from

- XILINX (XILINX Vertex II are recent devices)
- Actel, Altera and others

Floor-plan of VIRTEX II FPGAs

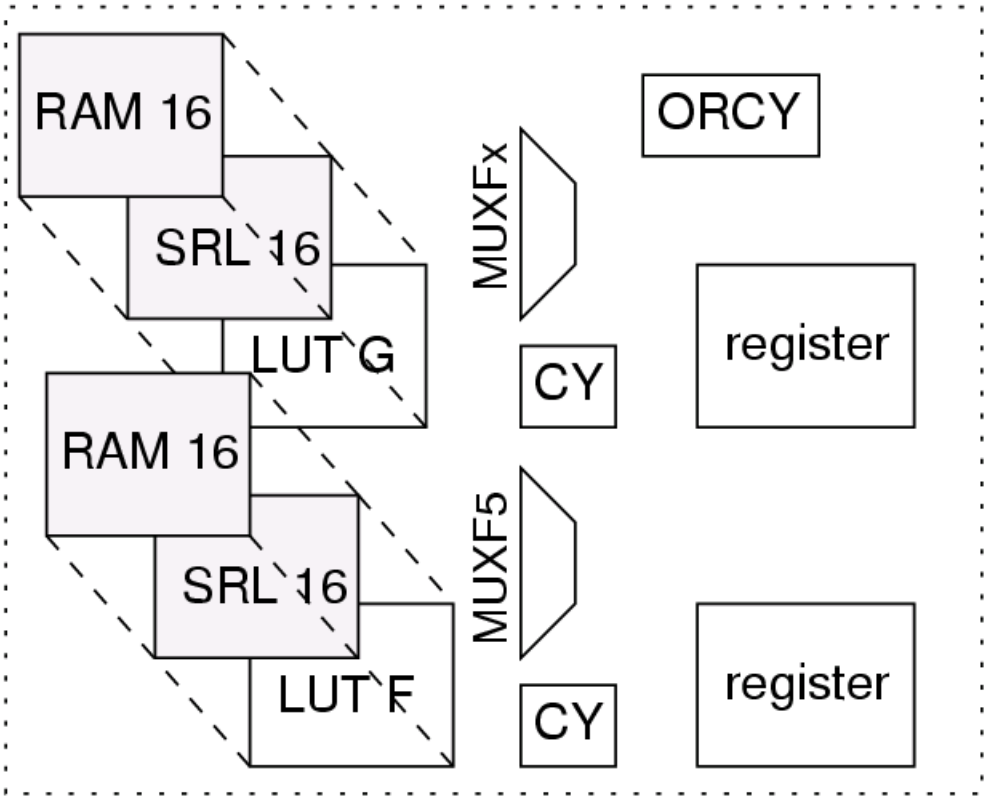


Virtex II Configurable Logic Block (CLB)



Virtex II Slice (simplified)

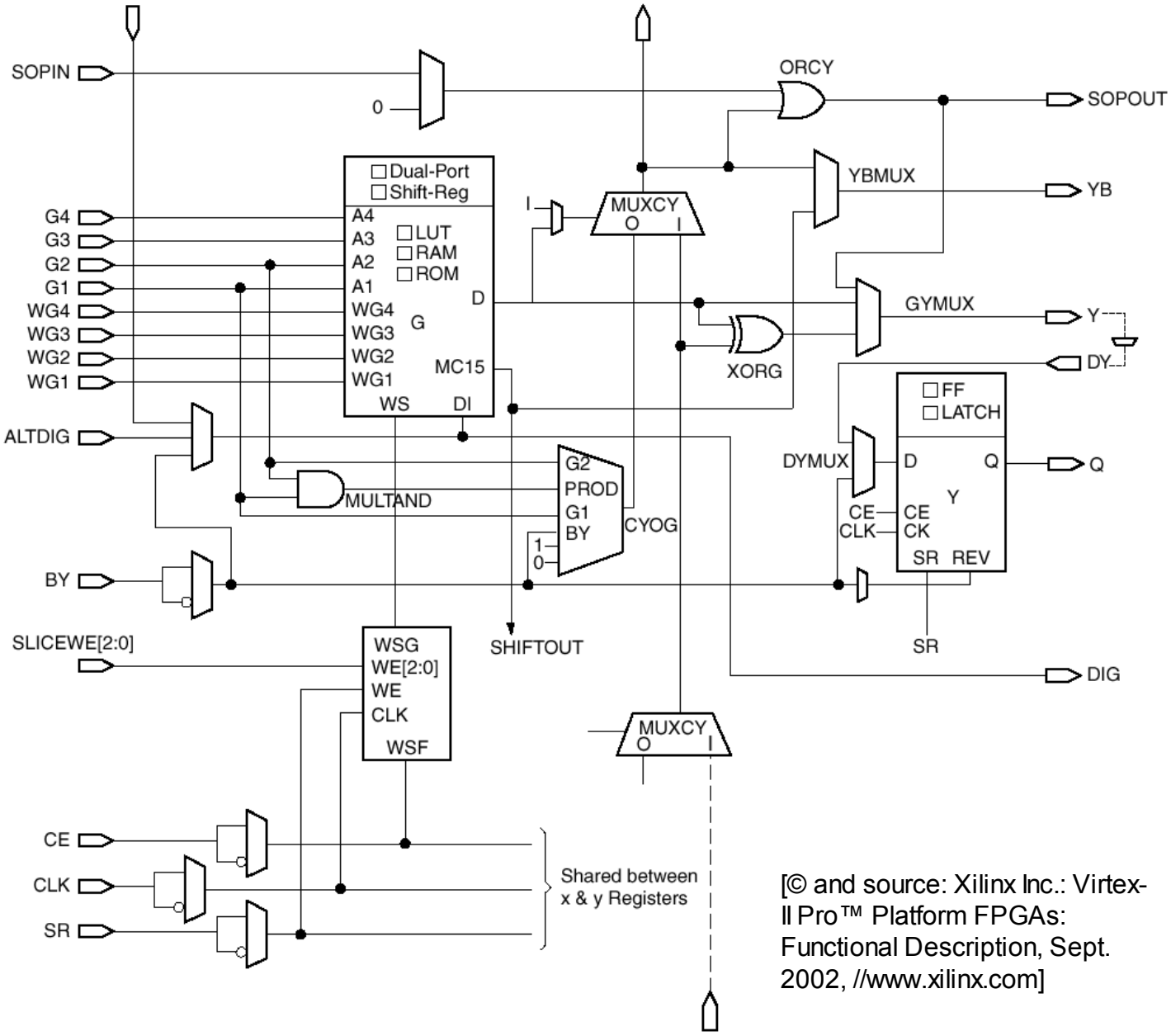
Look-up tables LUT F and G can be used to compute any Boolean function of ≤ 4 variables.



Example:

a	b	c	d	G
0	0	0	0	**0**
0	0	0	1	**1**
0	0	1	0	**1**
0	0	1	1	**0**
0	1	0	0	**1**
0	1	0	1	**0**
0	1	1	0	**0**
0	1	1	1	**1**
1	0	0	0	**1**
1	0	0	1	**0**
1	0	1	0	**0**
1	0	1	1	**1**
1	1	0	0	**0**
1	1	0	1	**1**
1	1	1	0	**1**
1	1	1	1	**0**

Virtex II (Pro) Slice



[© and source: Xilinx Inc.: Virtex-II Pro™ Platform FPGAs: Functional Description, Sept. 2002, //www.xilinx.com]

Number of resources available in Virtex II Pro devices

Table 16: **Virtex-II Pro Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM+ or Shift Register (bits)	Number of Flip-Flops	Number of Carry Chains(1)	Number of SOP Chains(1)
XC2VP2	16 x 22	1,408	2,816	45,056	2,816	44	32
XC2VP4	40 x 22	3,008	6,016	96,256	6,016	44	80
XC2VP7	40 x 34	4,928	9,856	157,696	9,856	68	80
XC2VP20	56 x 46	9,280	18,560	296,960	18,560	92	112
XC2VP30	80 x 46	13,696	27,392	438,272	27,392	92	160
XC2VP40	88 x 58	19,392	38,784	620,544	38,784	116	176
XC2VP50	88 x 70	23,616	47,232	755,712	47,232	140	176
XC2VP70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VP100	120 x 94	44,096	88,192	1,411,072	88,192	188	240
XC2VP125	136 x 106	55,616	111,232	1,779,712	111,232	212	272

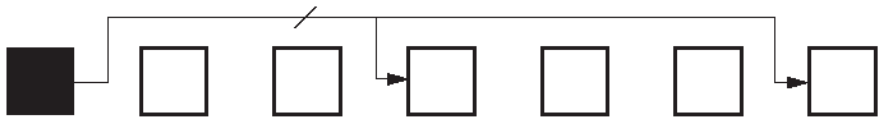
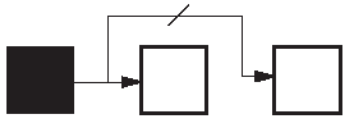
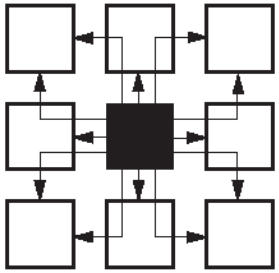
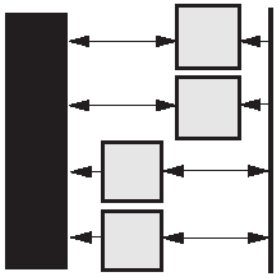
Notes:

1. The carry-chains and SOP chains can be split or cascaded.

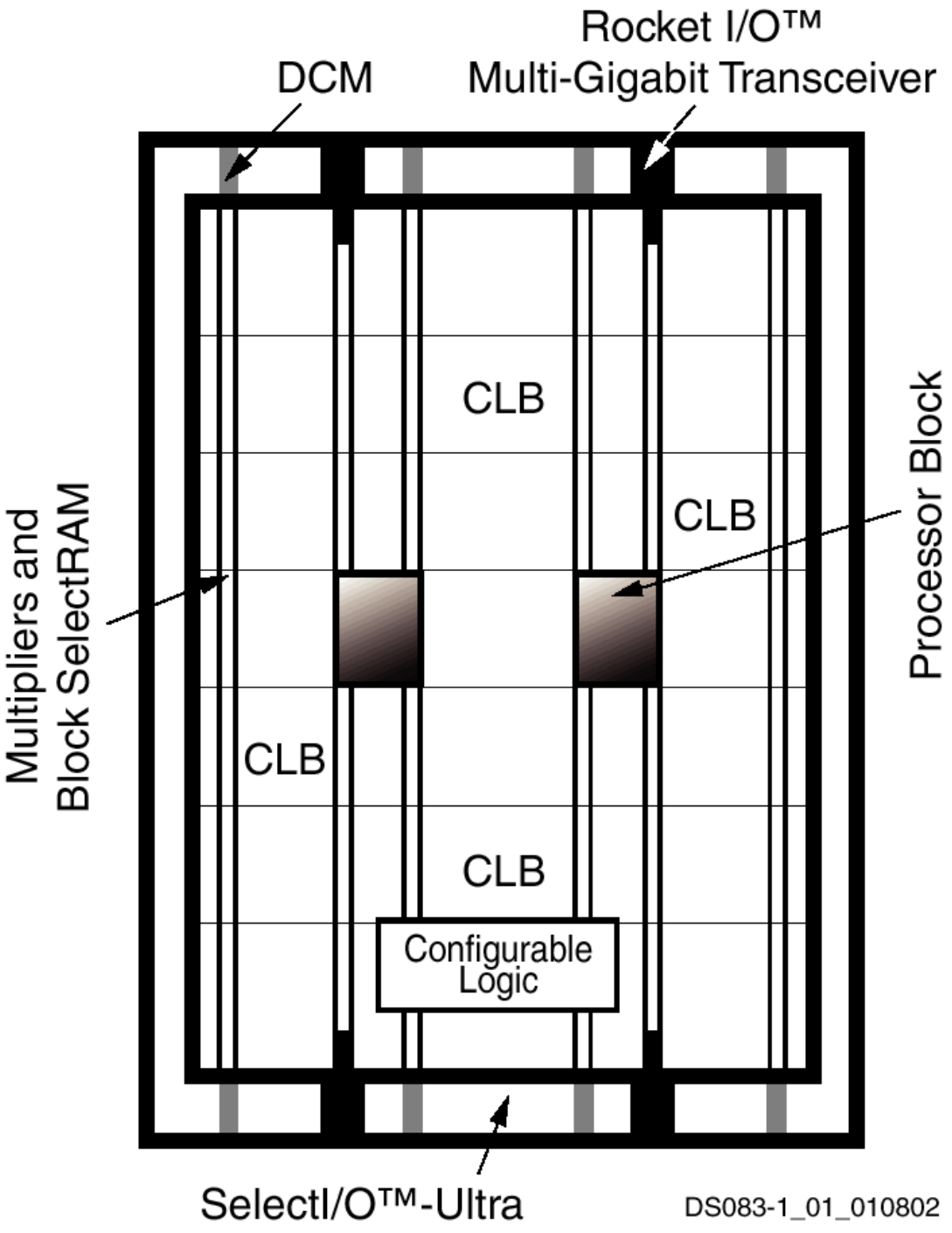
[© and source: Xilinx Inc.: Virtex-II Pro™ Platform FPGAs: Functional Description, Sept. 2002, //www.xilinx.com]

Interconnect

Hierarchical Routing Resources

24 Horizontal Long Lines 24 Vertical Long Lines	
120 Horizontal Hex Lines 120 Vertical Hex Lines	
40 Horizontal Double Lines 40 Vertical Double Lines	
16 Direct Connections (total in all four directions)	
8 Fast Connects	

Virtex II Pro Devices include up to 4 PowerPC processor cores



[© and source: Xilinx Inc.: Virtex-II Pro™ Platform FPGAs: Functional Description, Sept. 2002, //www.xilinx.com]

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Memory

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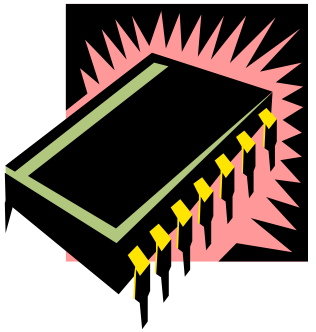
Memory

Memories?

Oops!
Memories!

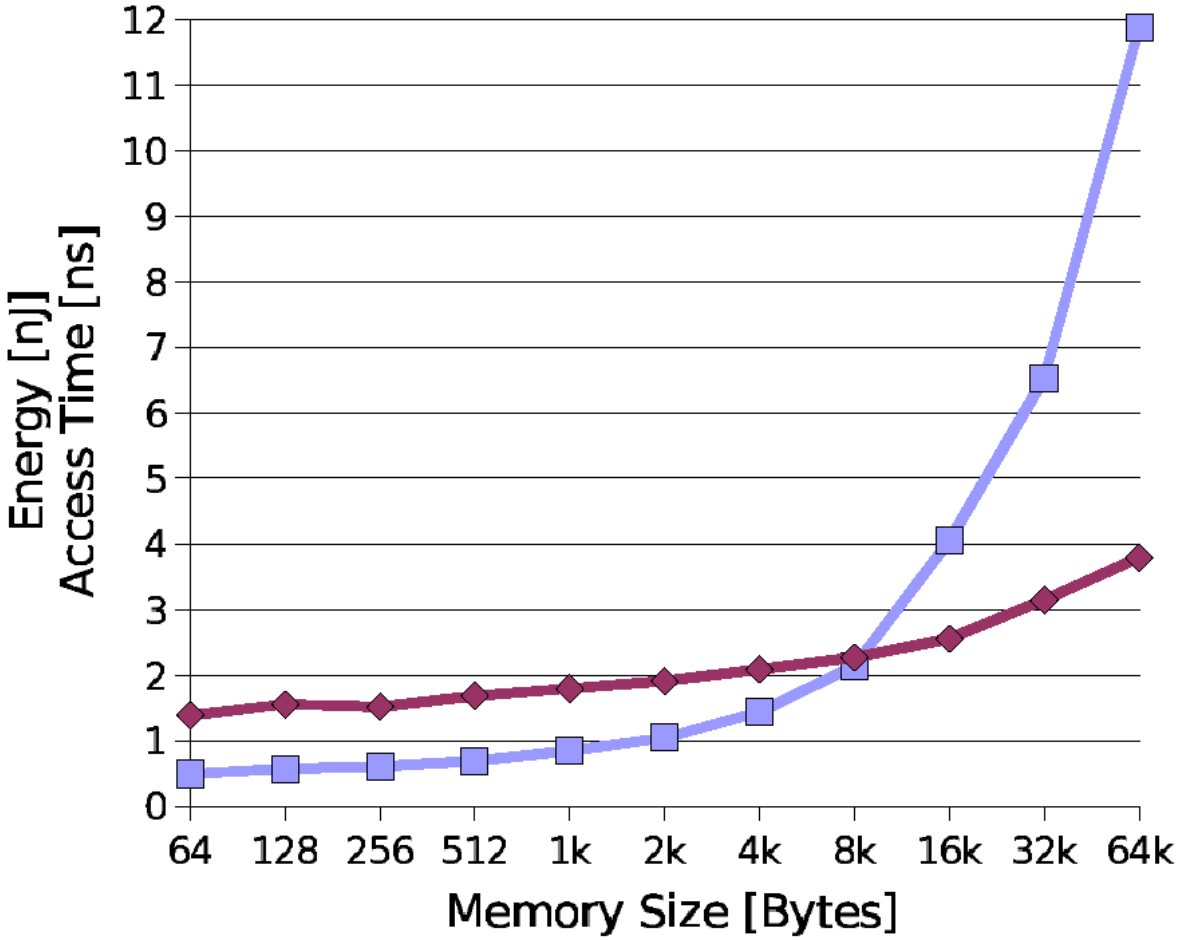


For the memory, efficiency is again a concern:

- speed (latency and throughput); predictable timing
- energy efficiency
- size
- cost
- other attributes (volatile vs. persistent, etc)

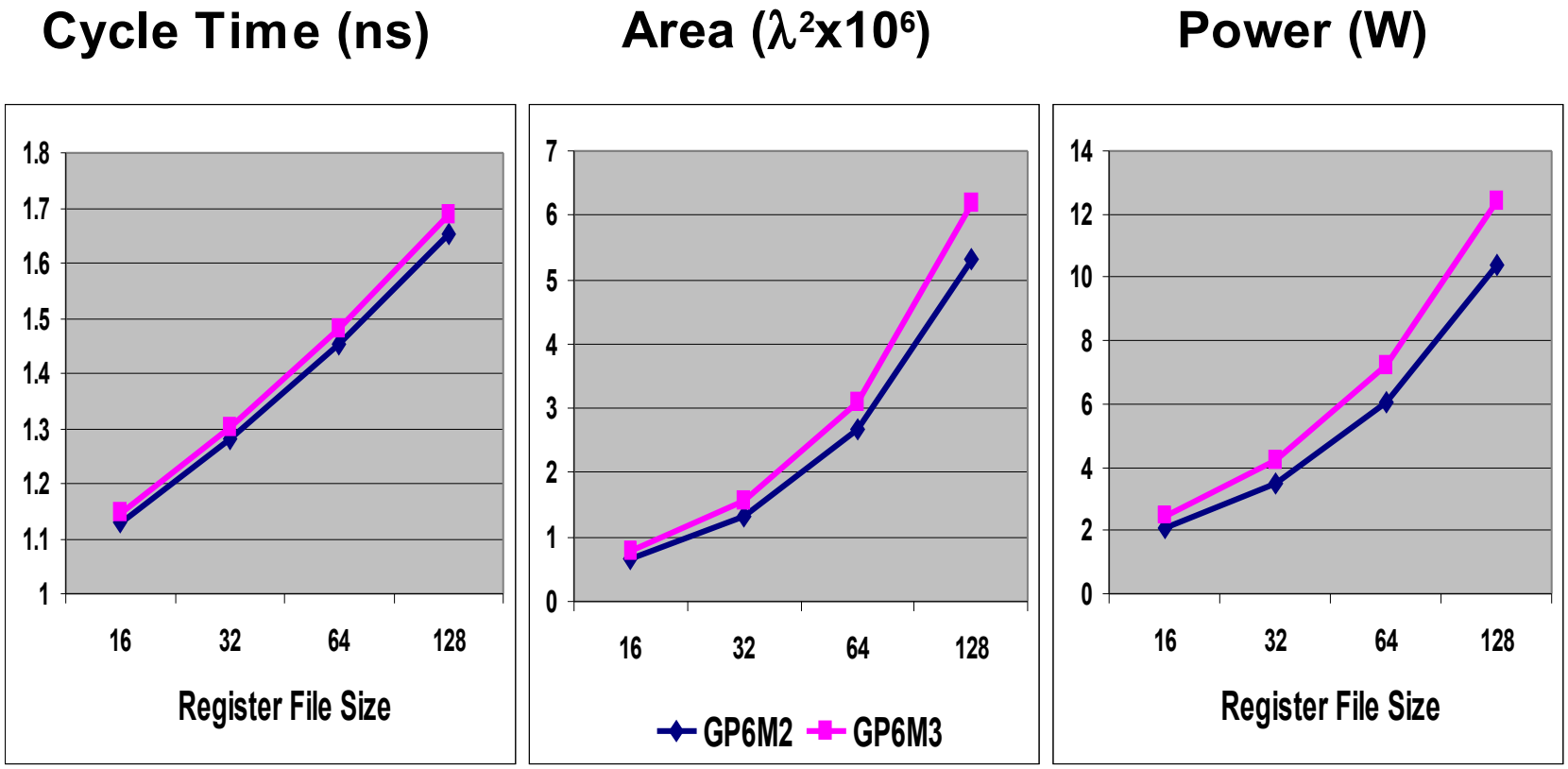
Access times and energy consumption increases with the size of the memory

Example (CACTI Model):



"Currently, the size of some applications is doubling every 10 months"
[STMicroelectronics, Medea+ Workshop, Stuttgart, Nov. 2003]

Access times and energy consumption for multi-ported register files

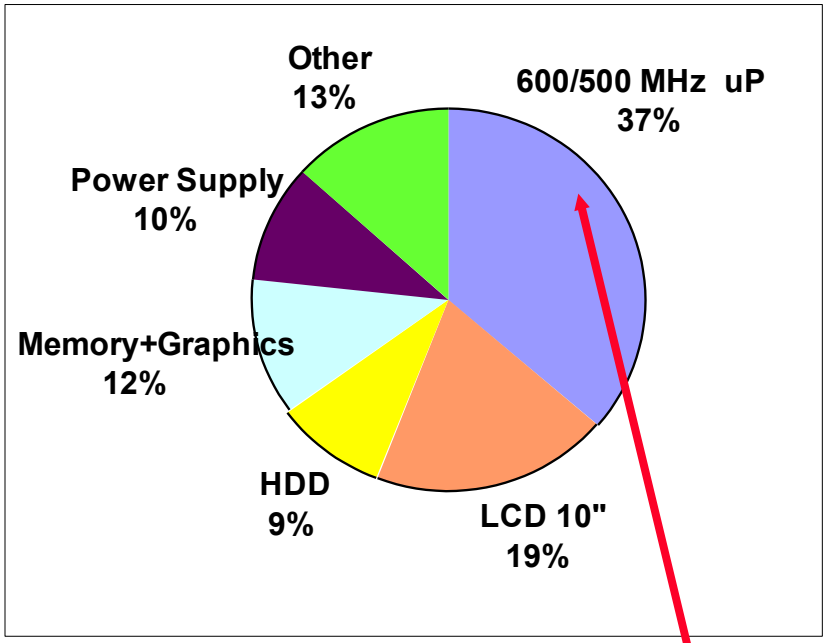


Rixner's et al. model [HPCA'00], Technology of 0.18 μm

Source and © H. Valero, 2001

How much of the energy consumption of a system is memory-related?

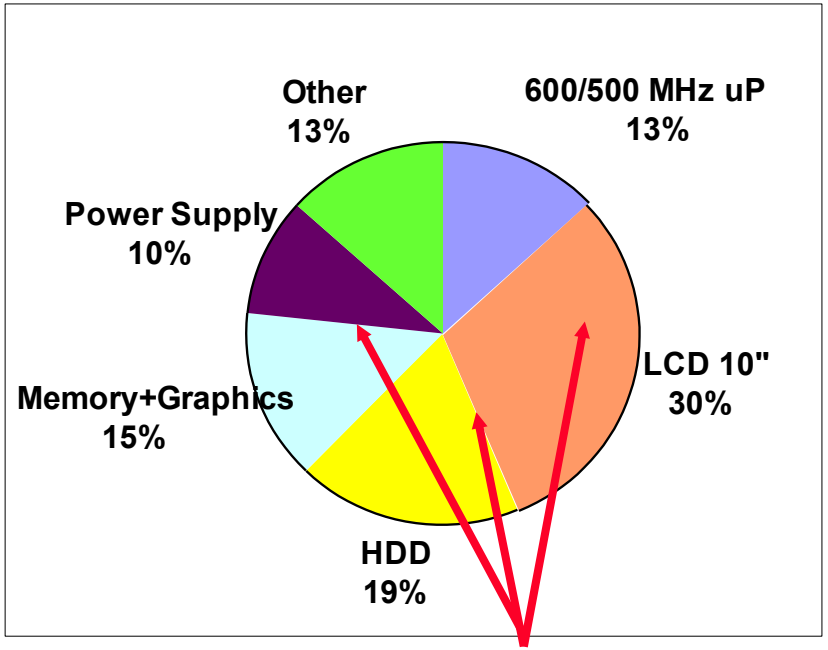
Mobile PC
Thermal Design (TDP) System Power



Note: Based on Actual Measurements

CPU Dominates Thermal Design Power

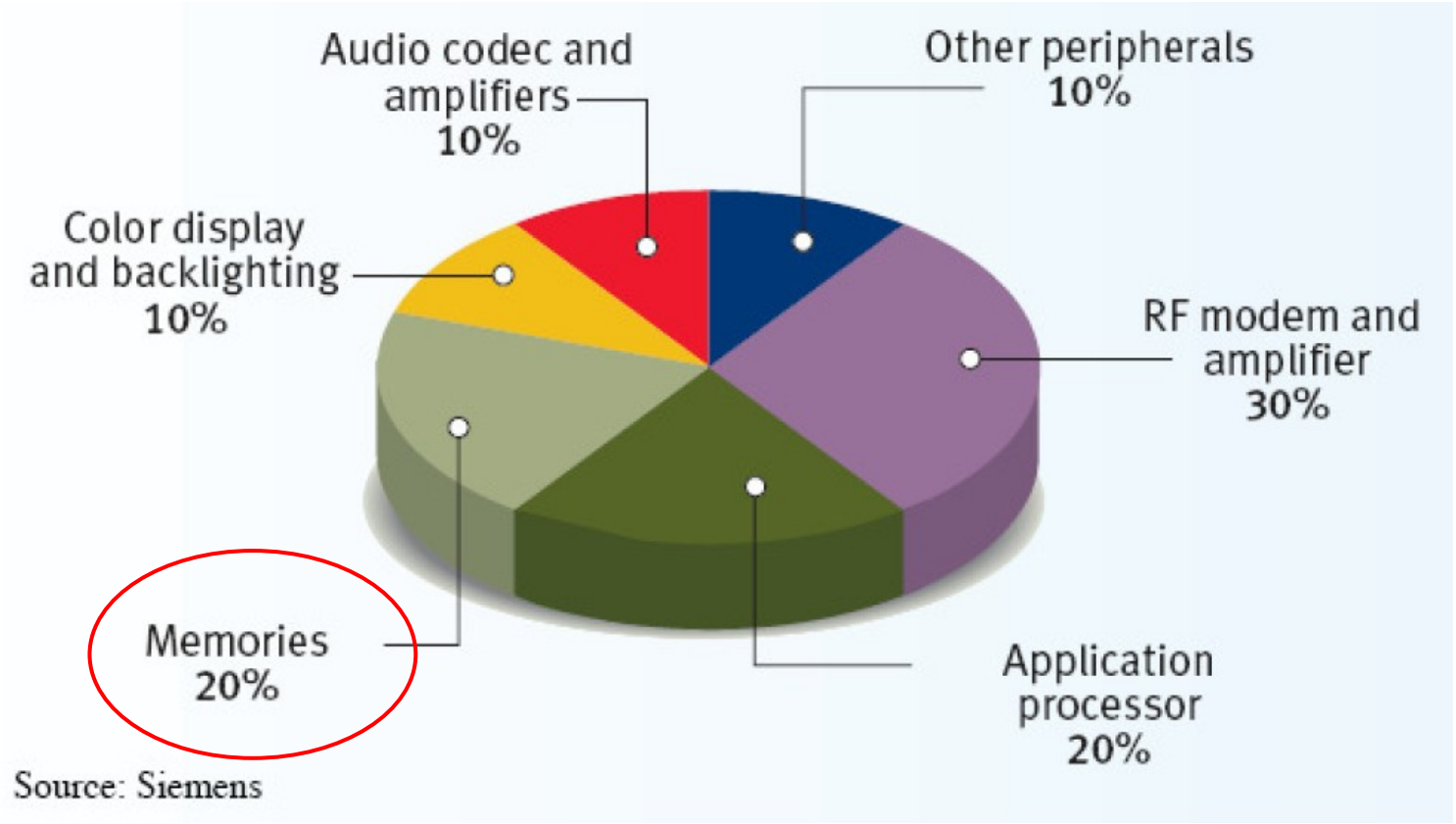
Mobile PC
Average System Power



Multiple Platform Components Comprise Average Power

[Courtesy: N. Dutt; Source: V. Tiwari]

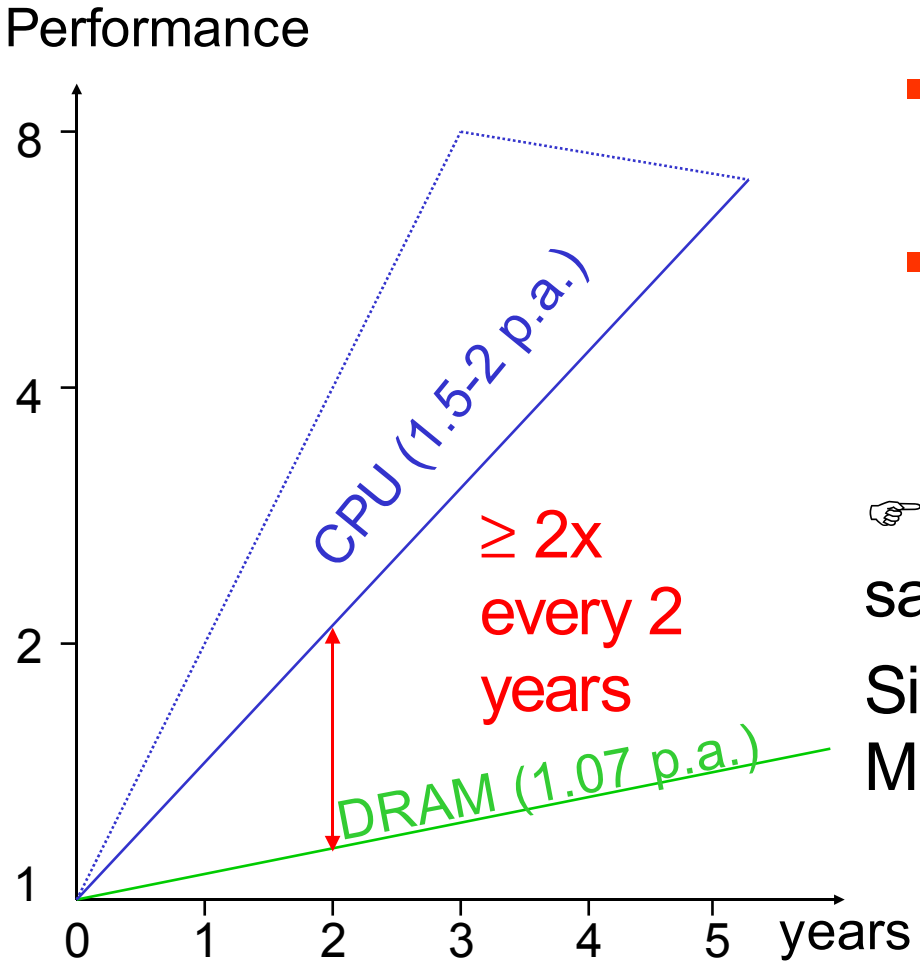
Energy consumption in mobile devices



[O. Vargas (Infineon Technologies): Minimum power consumption in mobile-phone memory subsystems; Pennwell Portable Design - September 2005;] Thanks to Thorsten Koch (Nokia/ Univ. Dortmund) for providing this source.

Access-times will be a problem

Speed gap between processing and main DRAM increases



- early 60ties (Atlas): page fault ~ 2500 instructions
- 2002 (2 GHz µP): access to DRAM ~ 500 instructions

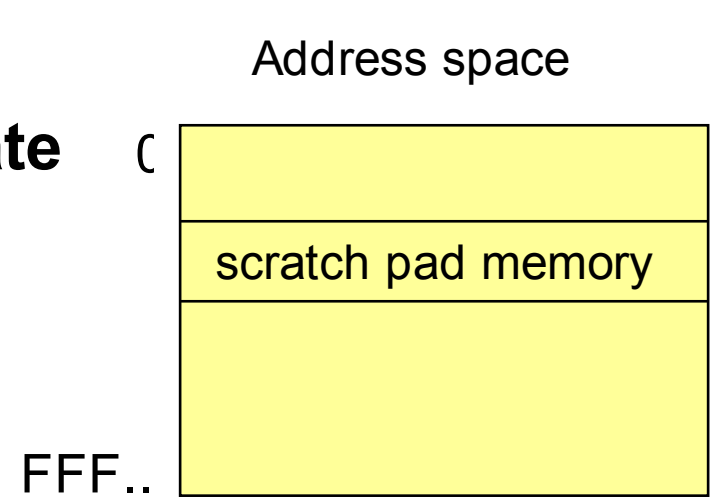
☞ penalty for cache miss about same as for page fault in Atlas

Similar problems for PCs and MPSoCs

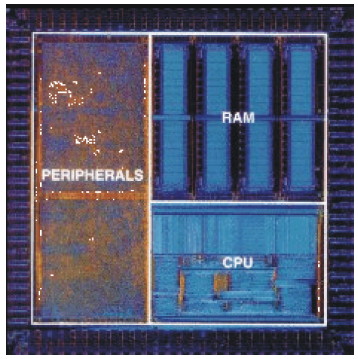
[P. Machanik: Approaches to Addressing the Memory Wall, TR Nov. 2002, U. Brisbane]

Hierarchical memories using scratch pad memories (SPM)

SPM is a small, physically separate memory mapped into the address space

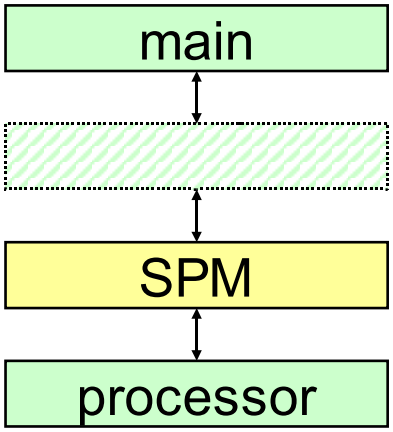


Example

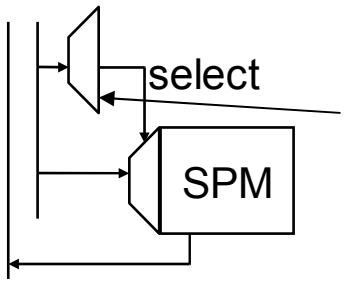


ARM7TDMI cores, well-known for low power consumption

Hierarchy



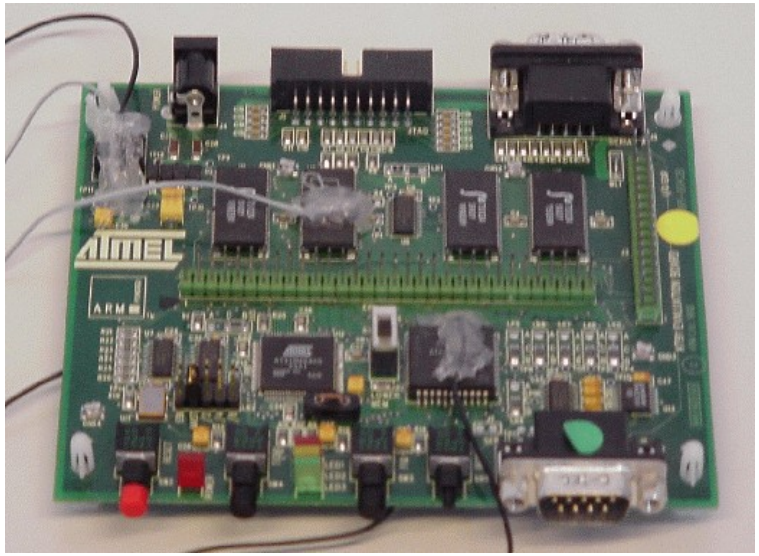
no tag memory

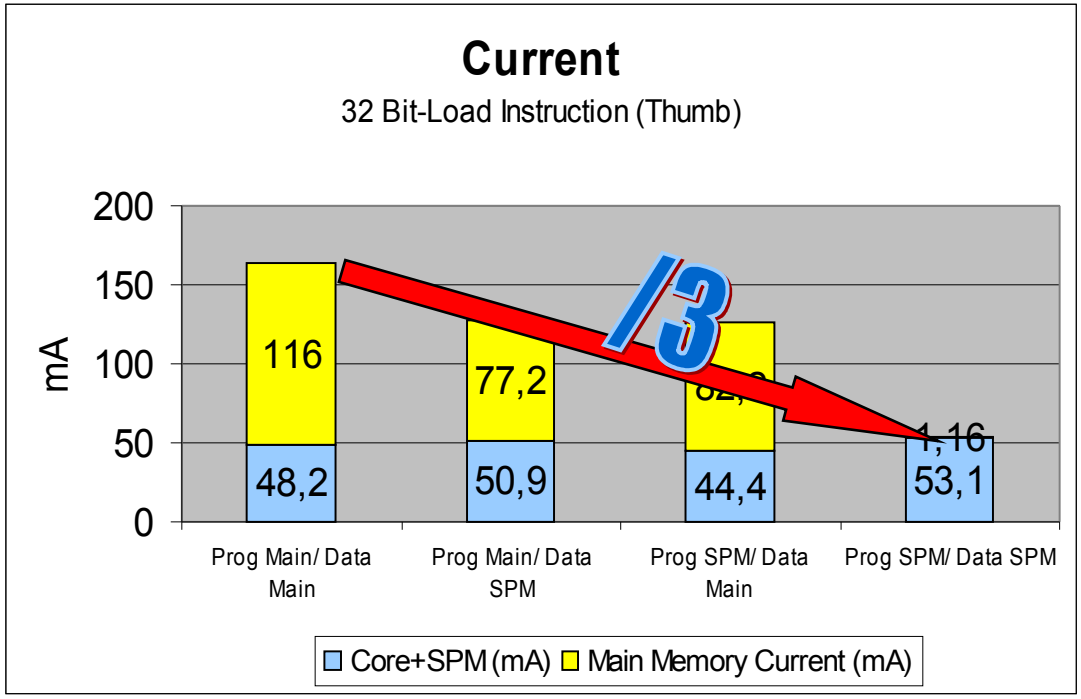


Selection is by an appropriate address decoder (simple!)

Comparison of currents using measurements

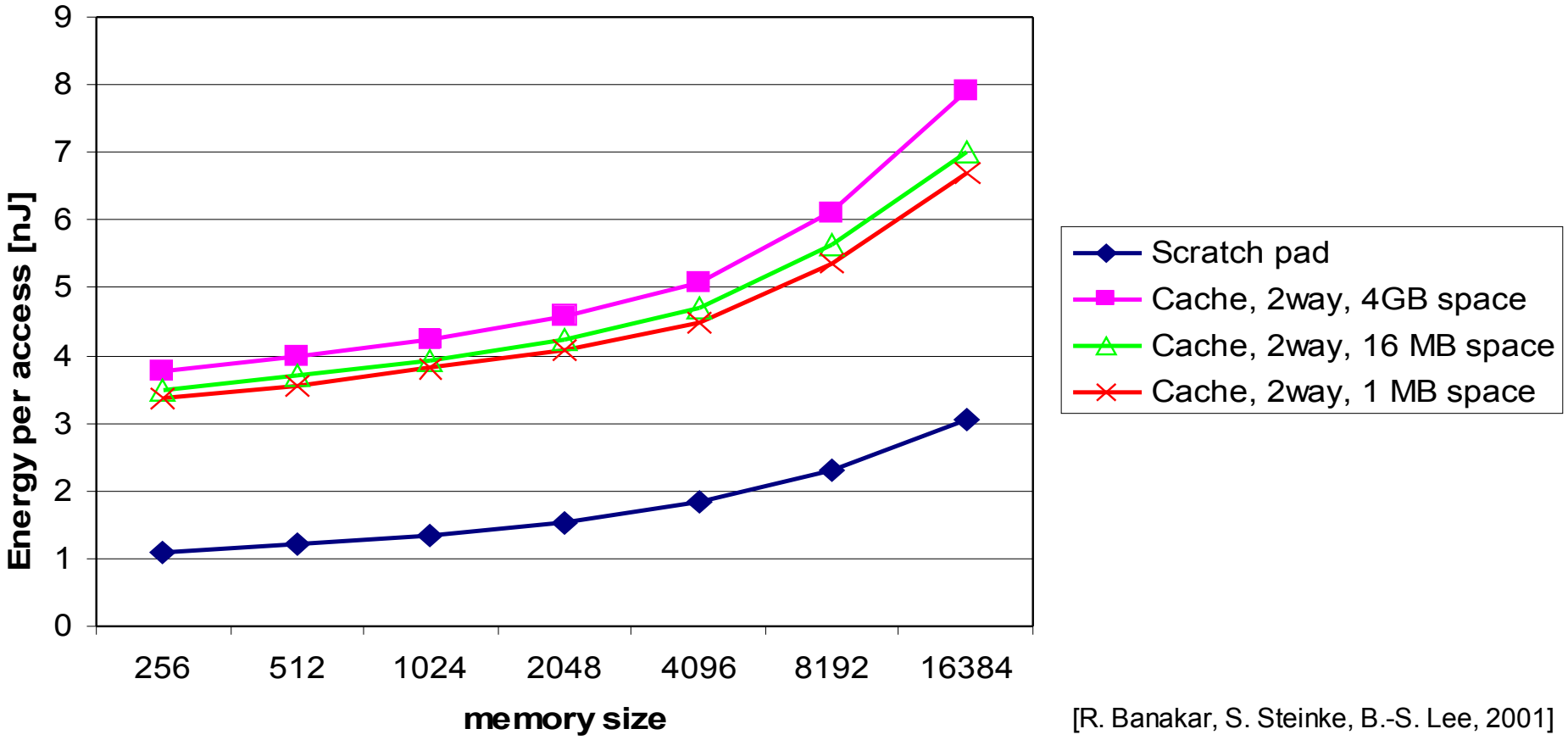
E.g.: ATMEL board with ARM7TDMI and ext. SRAM





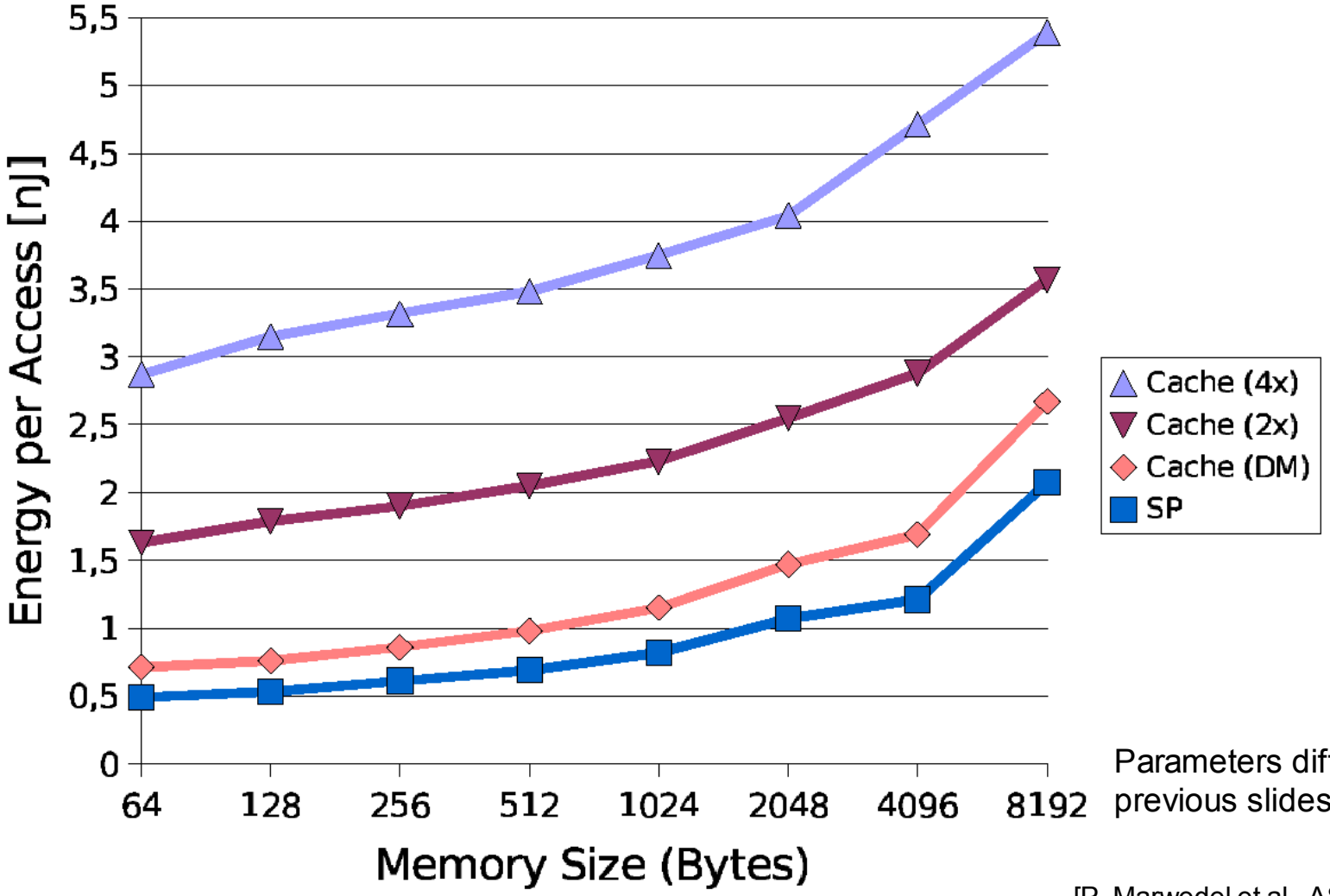
Why not just use a cache ? (1)

1. Energy for parallel access of sets, in comparators, muxes.



[R. Banakar, S. Steinke, B.-S. Lee, 2001]

Influence of the associativity



Parameters different from previous slides

[P. Marwedel et al., ASPDAC, 2004]

Communication

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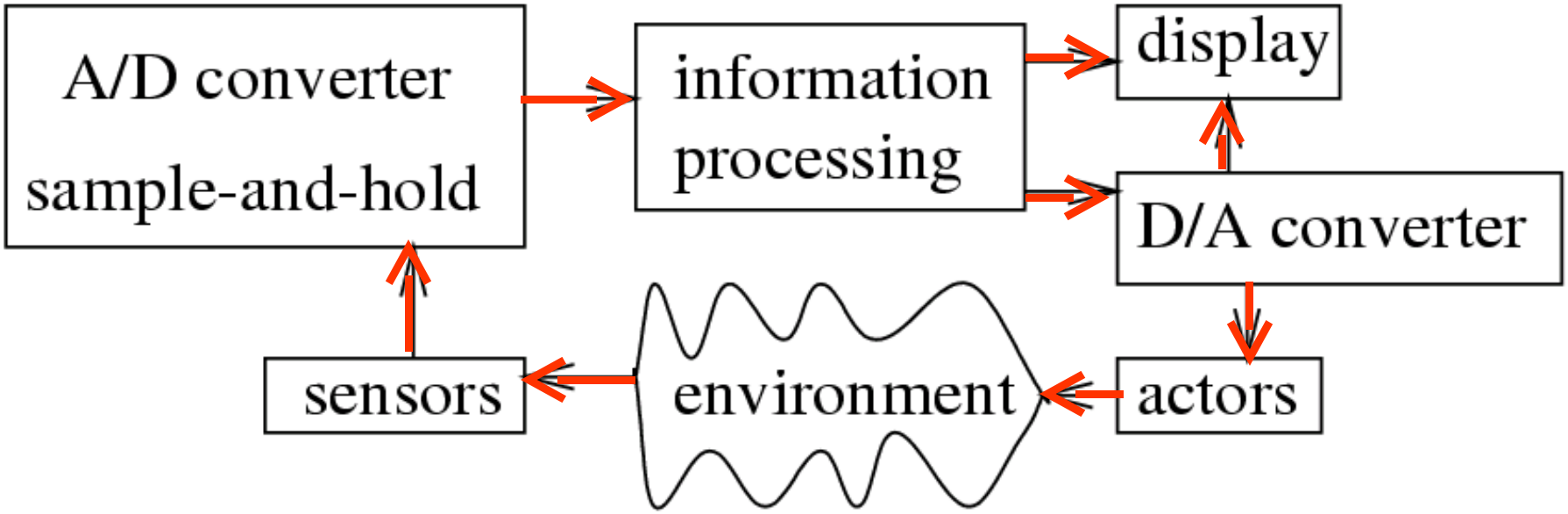
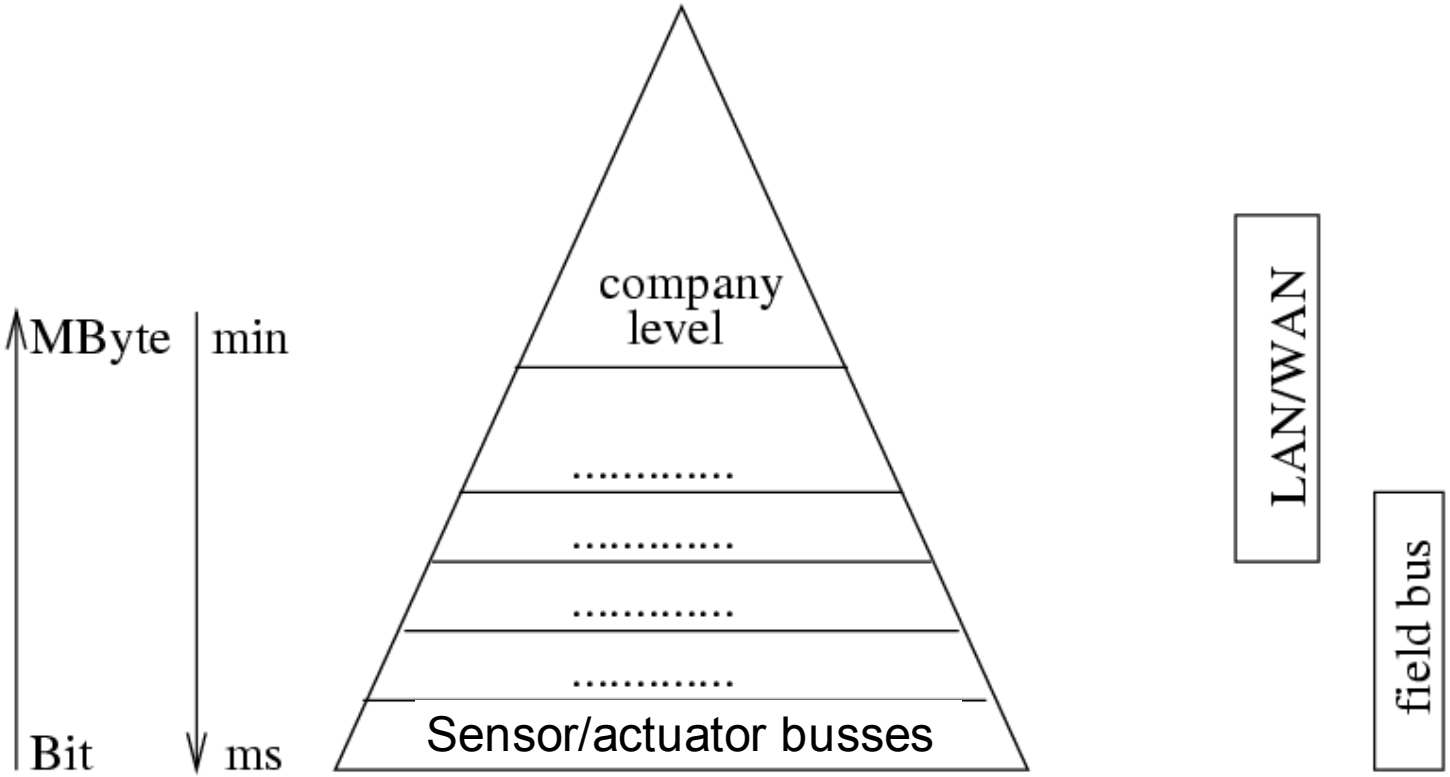
Communication



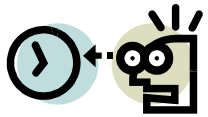
Communication: Hierarchy

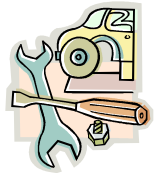
Inverse relation between volume and urgency quite common:



Communication
- Requirements -

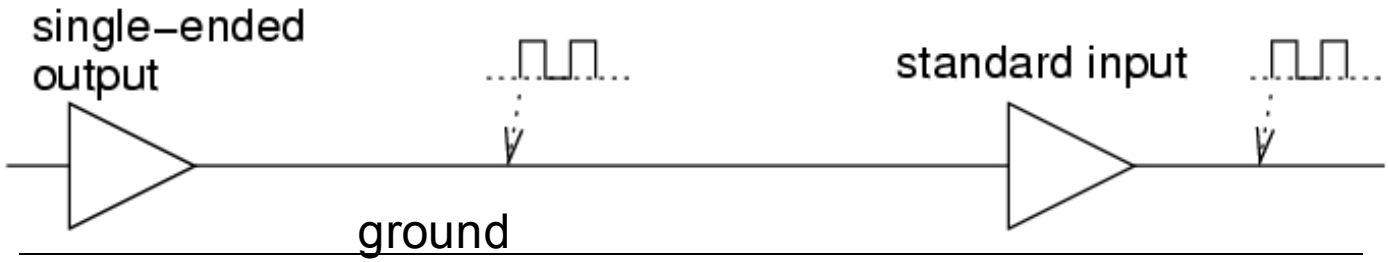
- Real-time behavior
- Efficient, economical
  (e.g. centralized power supply)
- Appropriate bandwidth and communication delay
- Robustness
- Fault tolerance
- Maintainability
- Diagnosability
- Security
- Safety



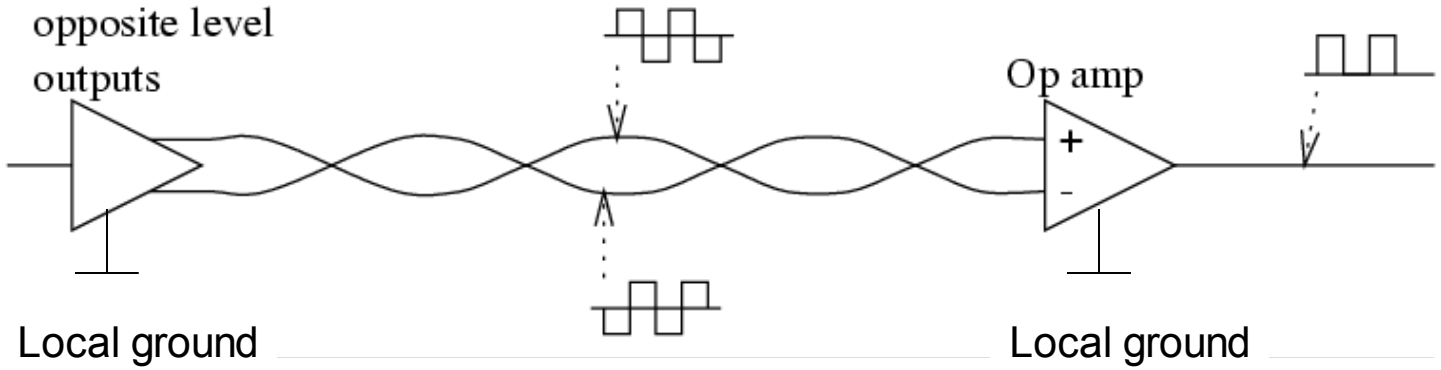


Basic techniques: Electrical robustness

Single-ended vs. differential signals



Voltage at input of Op-Amp positive → '1'; otherwise → '0'



Combined with twisted pairs; Most noise added to both wires.

Evaluation

Advantages:

- Subtraction removes most of the noise
- Changes of voltage levels have no effect
- Reduced importance of ground wiring
- Higher speed

Disadvantages:

- Requires negative voltages
- Increased number of wires and connectors

Applications:

- USB, FireWire, ISDN
- Ethernet (STP/UTP CAT 5 cables)
- differential SCSI
- High-quality analog audio signals

Real-time behavior

Carrier-sense multiple-access/collision-detection (CSMA/CD, Standard Ethernet) no guaranteed response time.
Alternatives:

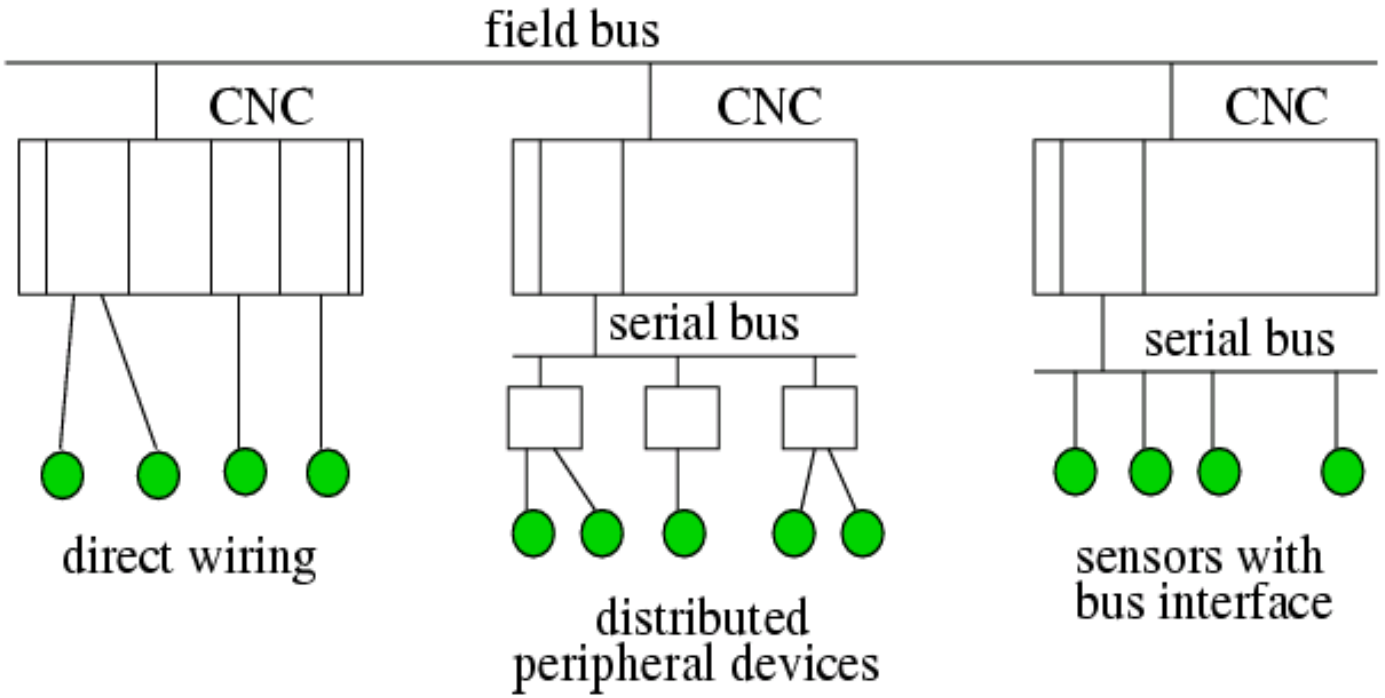
- token rings, token busses
- Carrier-sense multiple-access/collision-avoidance (CSMA/CA)
  - WLAN techniques with request preceding transmission
  - Each partner gets an ID (priority). After each bus transfer, all partners try setting their ID on the bus; partners detecting higher ID disconnect themselves from the bus. Highest priority partner gets guaranteed response time; others only if they are given a chance.

Other basic techniques

- **Fault tolerance:**
  error detecting and error correcting bus protocols
- **Privacy**:
  encryption, virtually private networks

Sensor/actuator busses

1. **Sensor/actuator busses**: Real-time behavior very important; different techniques:



Many wires less wires expensive & flexible

Field busses: Profibus

More powerful/expensive than sensor interfaces; mostly serial.
Emphasis on transmission of small number of bytes.
Examples:

1. **Process Field Bus (Profibus)**
   Designed for factory and process automation.
   Focus on **safety**; comprehensive protocol mechanisms.
   Claiming 20% market share for field busses.
   Token passing.
   ≦93.75 kbit/s (1200 m);1500 kbits/s (200m);
   12 Mbit/s (100m)
   Integration with Ethernet via Profinet.

[http://www.profibus.com/]

Controller area network (CAN)

2. Controller area network (CAN)

- Designed by Bosch and Intel in 1981;
- used in cars and other equipment;
- differential signaling with twisted pairs,
- arbitration using CSMA/CA,
- throughput between 10kbit/s and 1 Mbit/s,
- low and high-priority signals,
- maximum latency of 134 µs for high priority signals,
- coding of signals similar to that of serial (RS-232) lines of PCs, with modifications for differential signaling.
- See //www.can.bosch.com

Time-Triggered-Protocol (TTP)

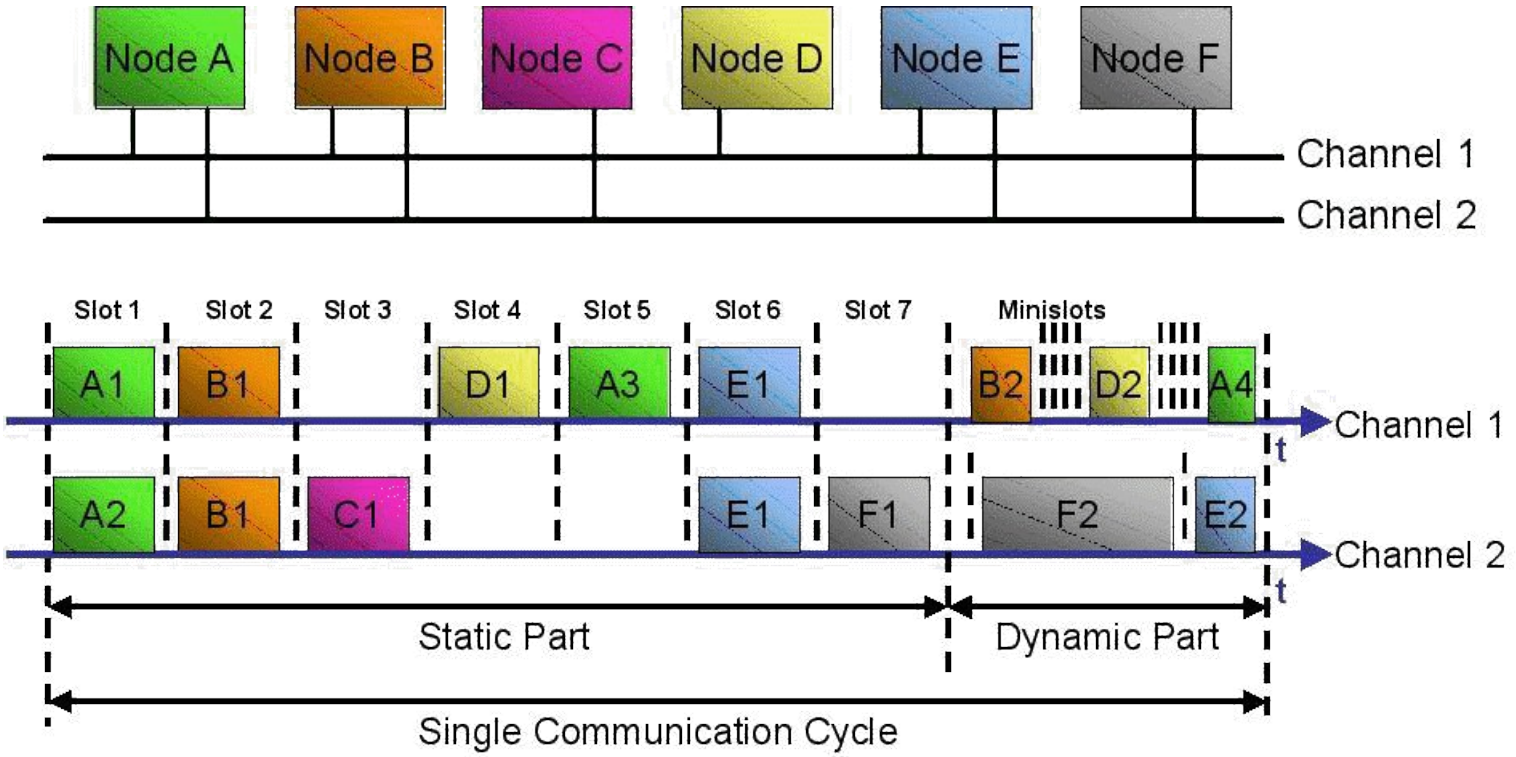
1. The **Time-Triggered-Protocol (TTP)** [Kopetz et al.] for fault-tolerant safety systems like airbags in cars.

FlexRay

1. **FlexRay**: developed by the FlexRay consortium (BMW, Ford, Bosch, DaimlerChrysler, …)
   Combination of a variant of the TTP and the Byteflight [Byteflight Consortium, 2003] protocol.
   Specified in SDL.
   - Improved error tolerance and time-determinism
   - Meets requirements with transfer rates >> CAN std.
     High data rate can be achieved:
     - initially targeted for ~ 10Mbit/sec;
     - design allows much higher data rates
   - TDMA (Time Division Multiple Access) protocol:
     Fixed time slot with exclusive access to the bus
   - Cycle subdivided into a static and a dynamic segment.

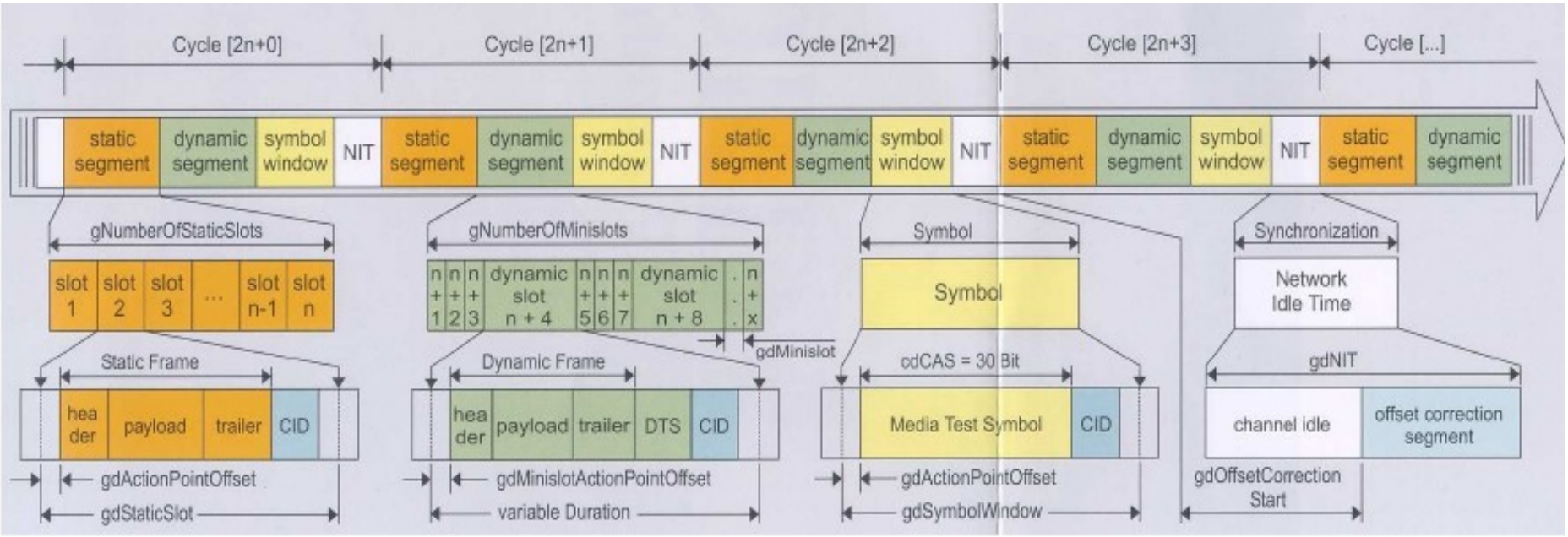
TDMA in FlexRay

Exclusive bus access enabled for short time in each case.
Dynamic segment for transmission of variable length information.
Fixed priorities in dynamic segment: Minislots for each potential sender.
Bandwidth used only when it is actually needed.



http://www.tzm.de/FlexRay/FlexRay_Introduction.html

Time intervals in Flexray

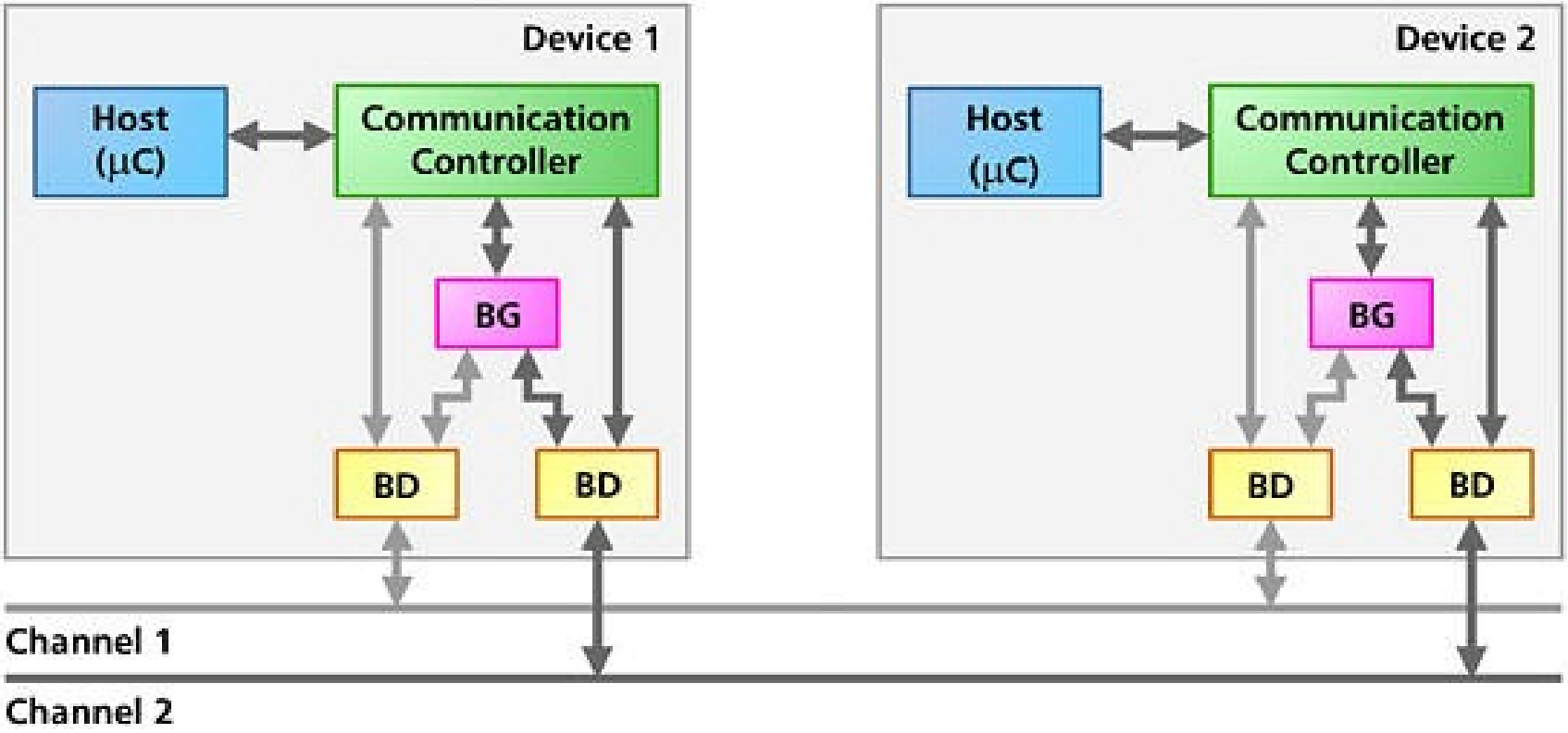


Quelle: Vector Informatik GmbH

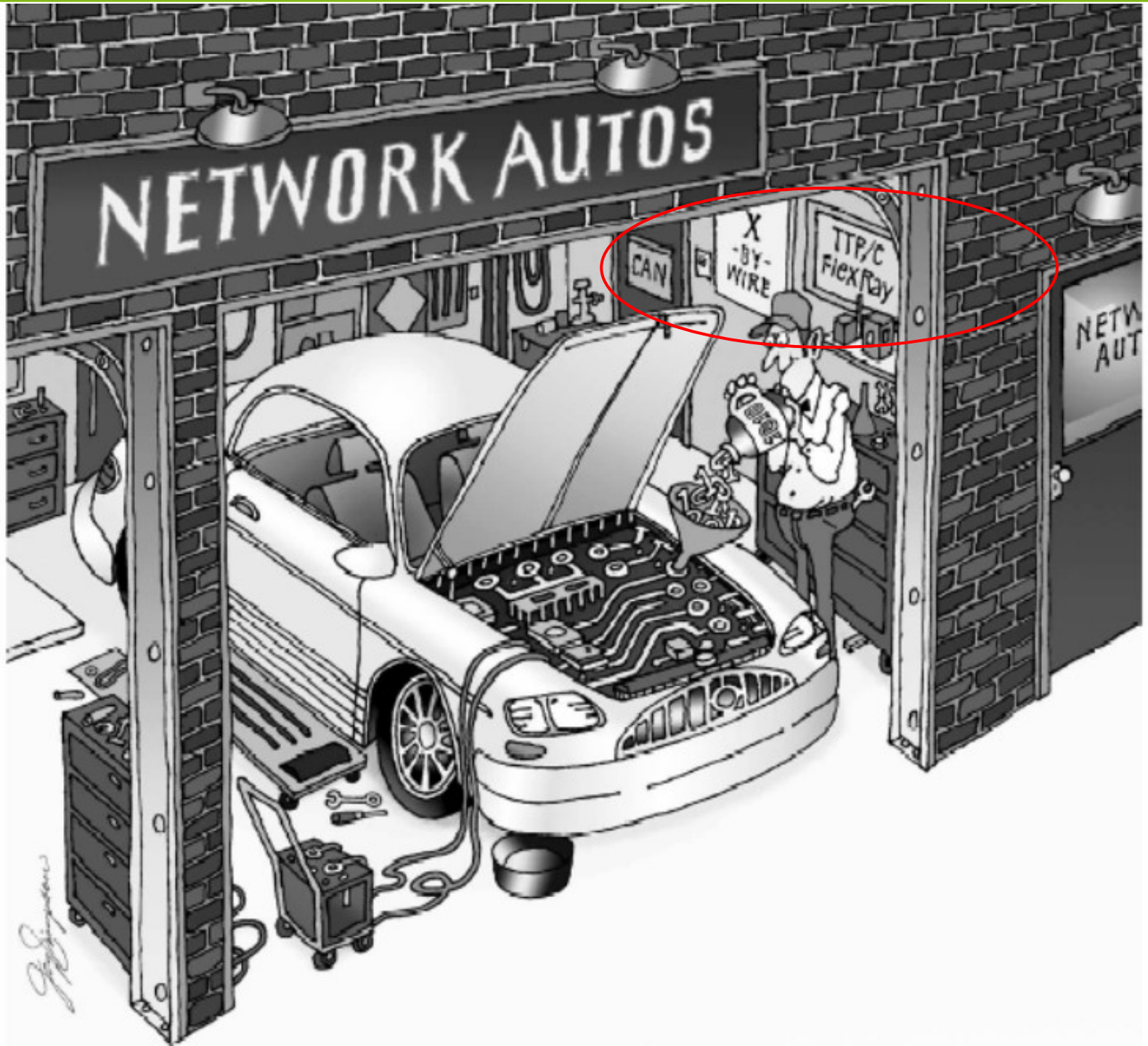
- **Microtick (*μt*)** = Clock period in partners, may differ between partners
- **Macrotick (*mt*)** = Basic unit of time, synchronized between partners (=$r_i \times \mu t$, r_i varies between partners *i*)
- **Slot**=Interval allocated per sender in static segment (=$p \times mt$, *p*: fixed (configurable))
- **Minislot** = Interval allocated per sender in dynamic segment (=$q \times mt$, *q*: variable) Short minislot if no transmission needed; starts after previous minislot.
- **Cycle** = Static segment + dynamic segment + network idle time

Structure of Flexray networks

Bus guardian protects the system against failing processors, e.g. so-called “babbling idiots”



http://www.ixxat.de/index.php?seite=introduction_flexray_en&root=5873&system_id=5875&com=formular_suche_treffer&markierung=flexray



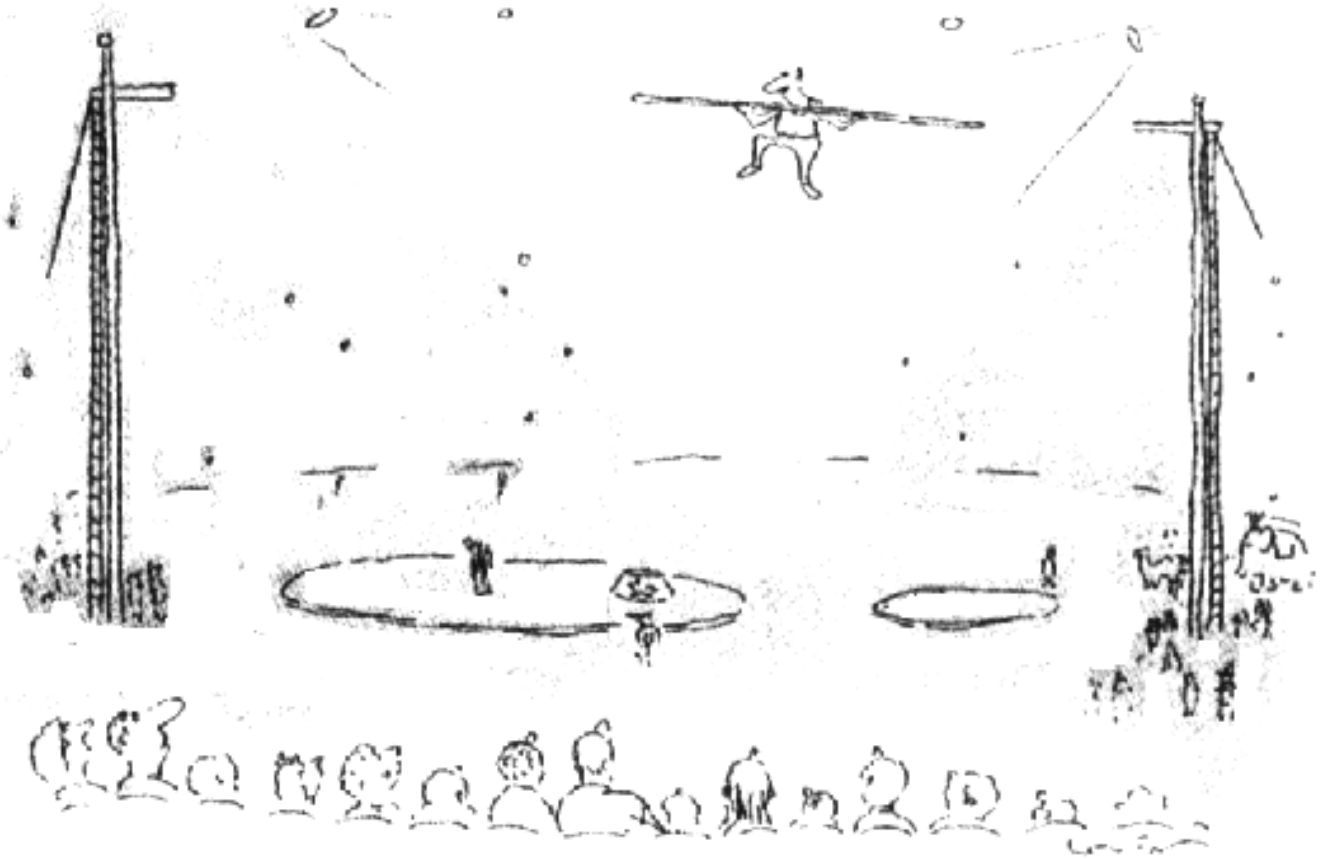
FlexRay™

http://www.computer.org/micro/mi2002/pdf/m4010.pdf

Other field busses

- **LIN**
- **MAP:**MAP is a bus designed for car factories.
- **EIB:**The European Installation Bus (EIB) is a bus designed for smart homes. **European Installation Bus (EIB)**
  Designed for smart buildings; CSMA/CA; low data rate.
- **IEEE 488:** Designed for laboratory equipment.
- Attempts to use standard Ethernet.
  However, timing predictability remains a serious issue.

Wireless communication



"It appears to be some new kind of wireless technology."

Wireless communication: Examples

- IEEE 802.11 a/b/g/n
- UMTS
- DECT
- Bluetooth
- ZigBee

Timing predictability of wireless communication?

Summary

- FPGAs
- Memories
  - “Small is beautiful”
    (in terms of energy consumption, access times, size)
- Communication structures