Embedded System Hardware
- Reconfigurable Hardware -

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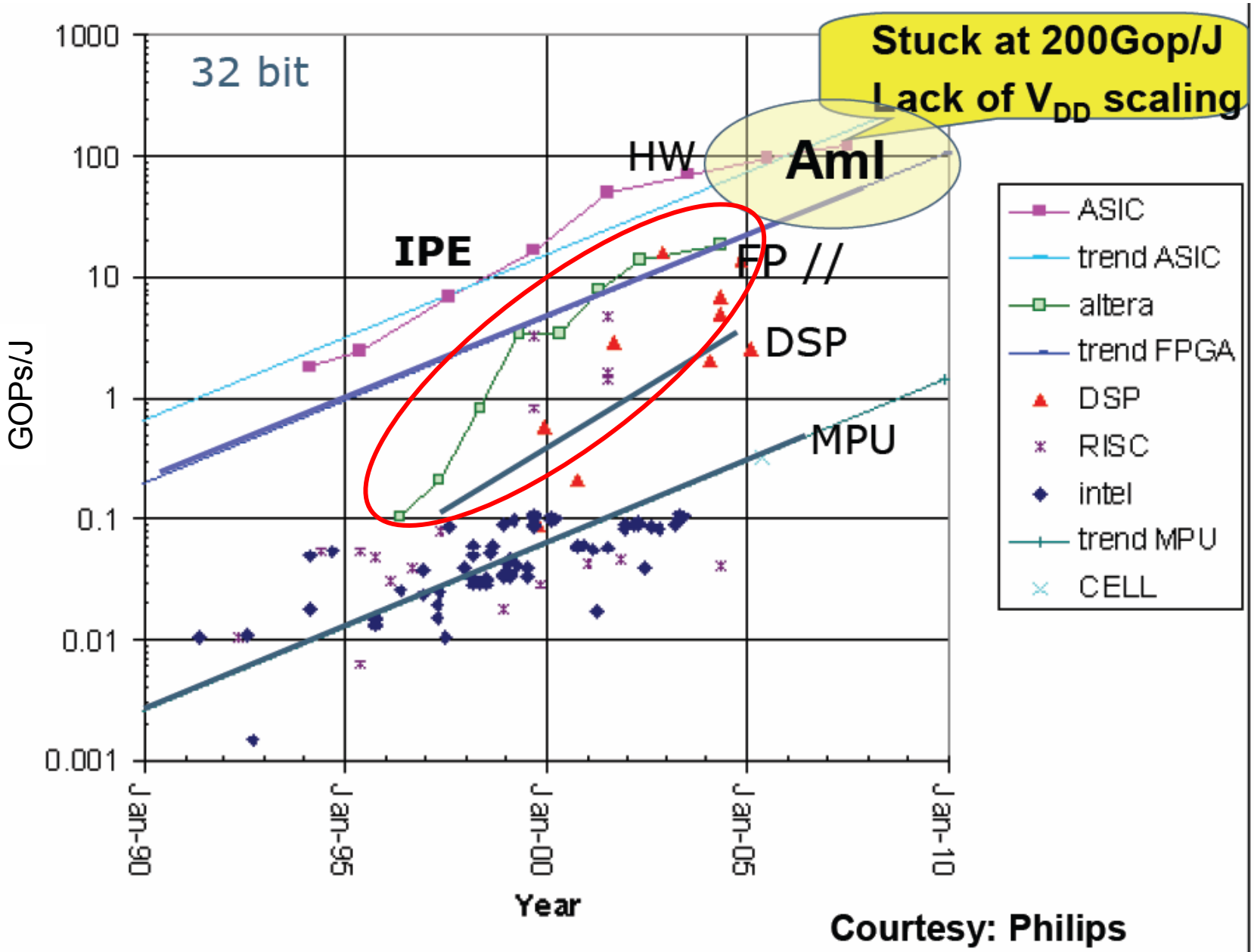
Energy Efficiency of FPGAs



Courtesy: Philips
© Hugo De Man, IMEC, 2007

Reconfigurable Logic

Full custom chips may be too expensive, software too slow.

Combine the speed of HW with the flexibility of SW

- ☞HW with programmable functions and interconnect.
- ☞Use of configurable hardware;
  common form: field programmable gate arrays (FPGAs)

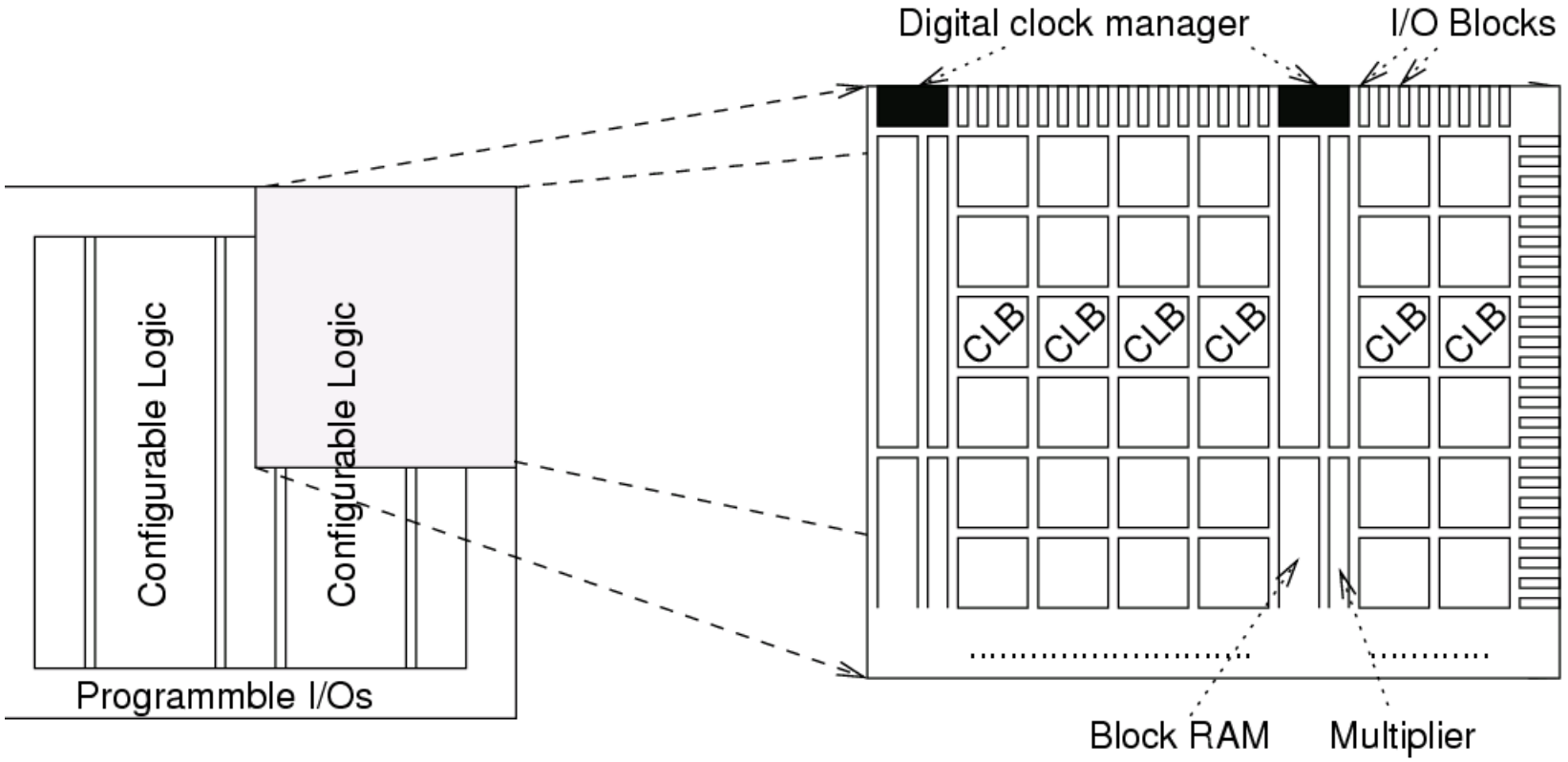
Applications: bit-oriented algorithms like

- encryption,
- fast “object recognition“ (medical and military)
- Adapting mobile phones to different standards.

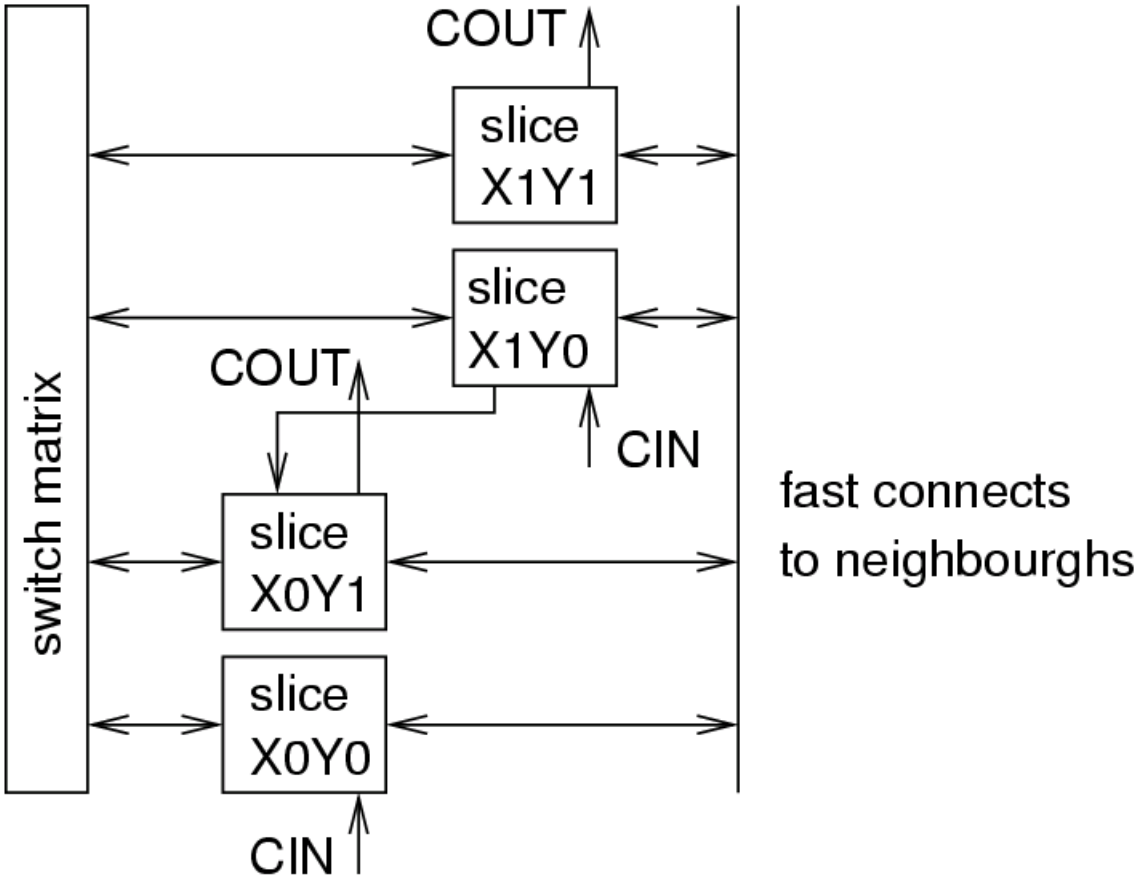
Very popular devices from

- XILINX (XILINX Vertex II are recent devices)
- Actel, Altera and others

Floor-plan of VIRTEX II FPGAs

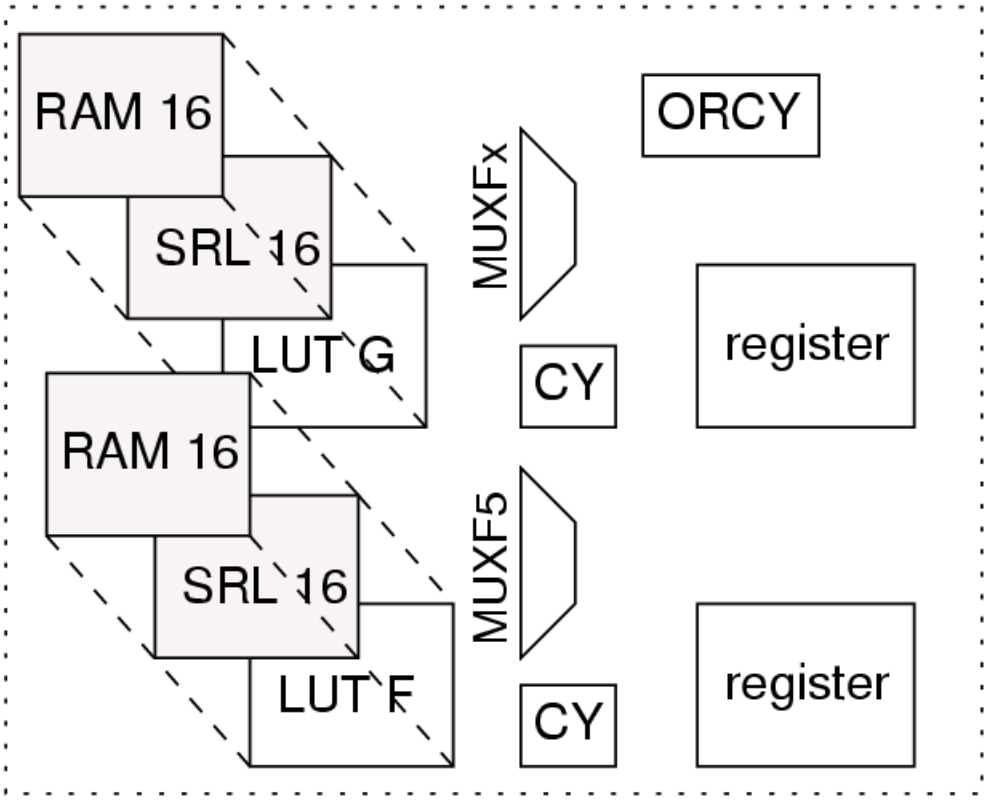


Virtex II Configurable Logic Block (CLB)



Virtex II Slice (simplified)

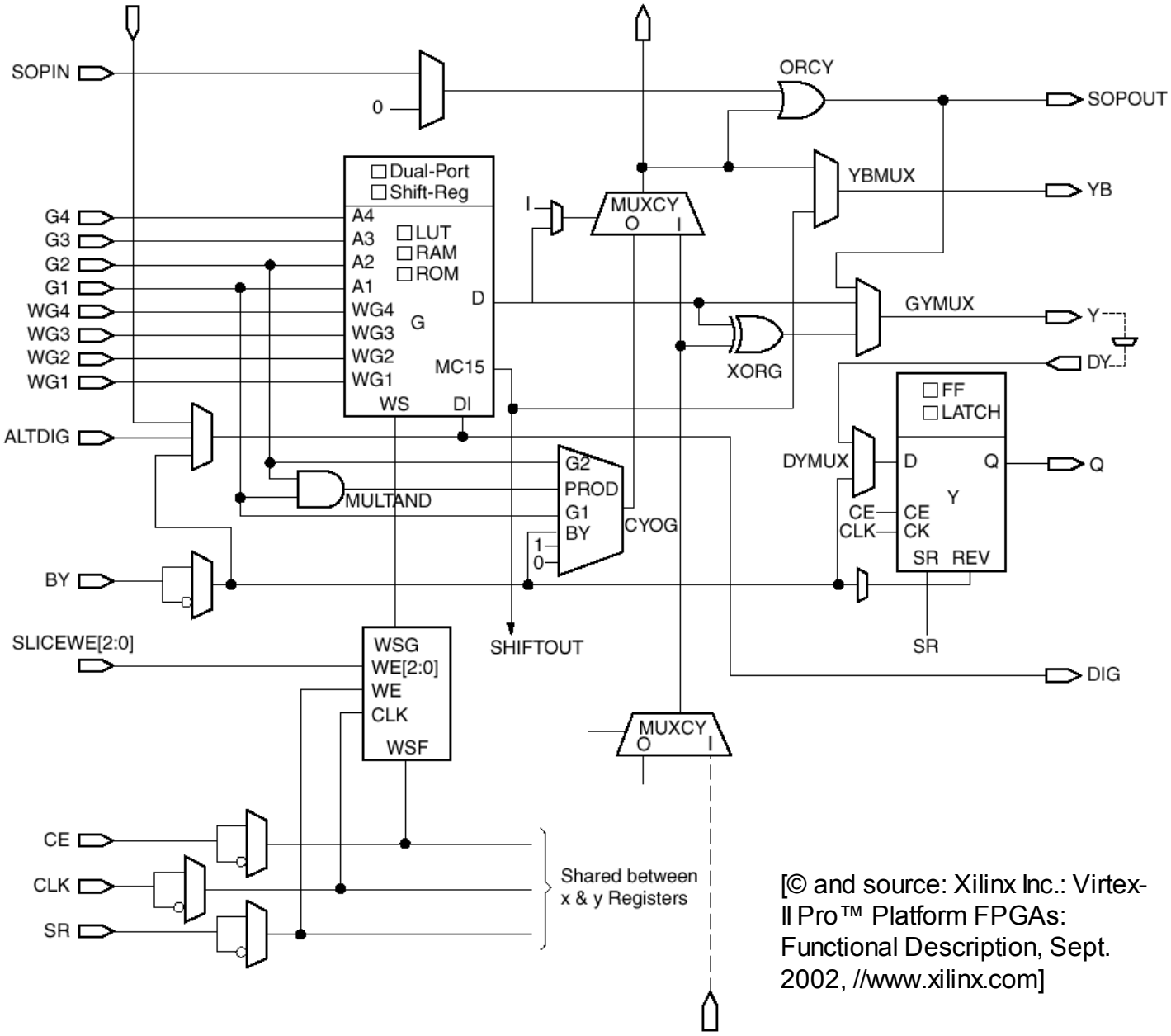
Look-up tables LUT F and G can be used to compute any Boolean function of ≤ 4 variables.



Example:

a	b	c	d	G
0	0	0	0	**0**
0	0	0	1	**1**
0	0	1	0	**1**
0	0	1	1	**0**
0	1	0	0	**1**
0	1	0	1	**0**
0	1	1	0	**0**
0	1	1	1	**1**
1	0	0	0	**1**
1	0	0	1	**0**
1	0	1	0	**0**
1	0	1	1	**1**
1	1	0	0	**0**
1	1	0	1	**1**
1	1	1	0	**1**
1	1	1	1	**0**

Virtex II (Pro) Slice



[© and source: Xilinx Inc.: Virtex-II Pro™ Platform FPGAs: Functional Description, Sept. 2002, //www.xilinx.com]

Number of resources available in Virtex II Pro devices

Table 16: **Virtex-II Pro Logic Resources Available in All CLBs**

Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM+ or Shift Register (bits)	Number of Flip-Flops	Number of Carry Chains(1)	Number of SOP Chains(1)
XC2VP2	16 x 22	1,408	2,816	45,056	2,816	44	32
XC2VP4	40 x 22	3,008	6,016	96,256	6,016	44	80
XC2VP7	40 x 34	4,928	9,856	157,696	9,856	68	80
XC2VP20	56 x 46	9,280	18,560	296,960	18,560	92	112
XC2VP30	80 x 46	13,696	27,392	438,272	27,392	92	160
XC2VP40	88 x 58	19,392	38,784	620,544	38,784	116	176
XC2VP50	88 x 70	23,616	47,232	755,712	47,232	140	176
XC2VP70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VP100	120 x 94	44,096	88,192	1,411,072	88,192	188	240
XC2VP125	136 x 106	55,616	111,232	1,779,712	111,232	212	272

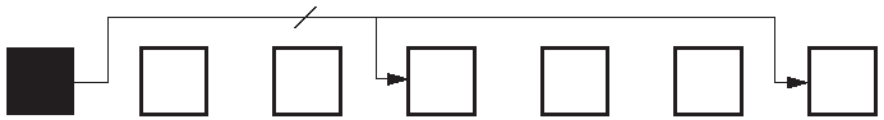
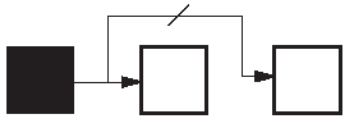
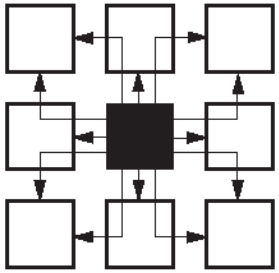
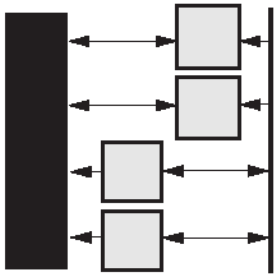
Notes:

1. The carry-chains and SOP chains can be split or cascaded.

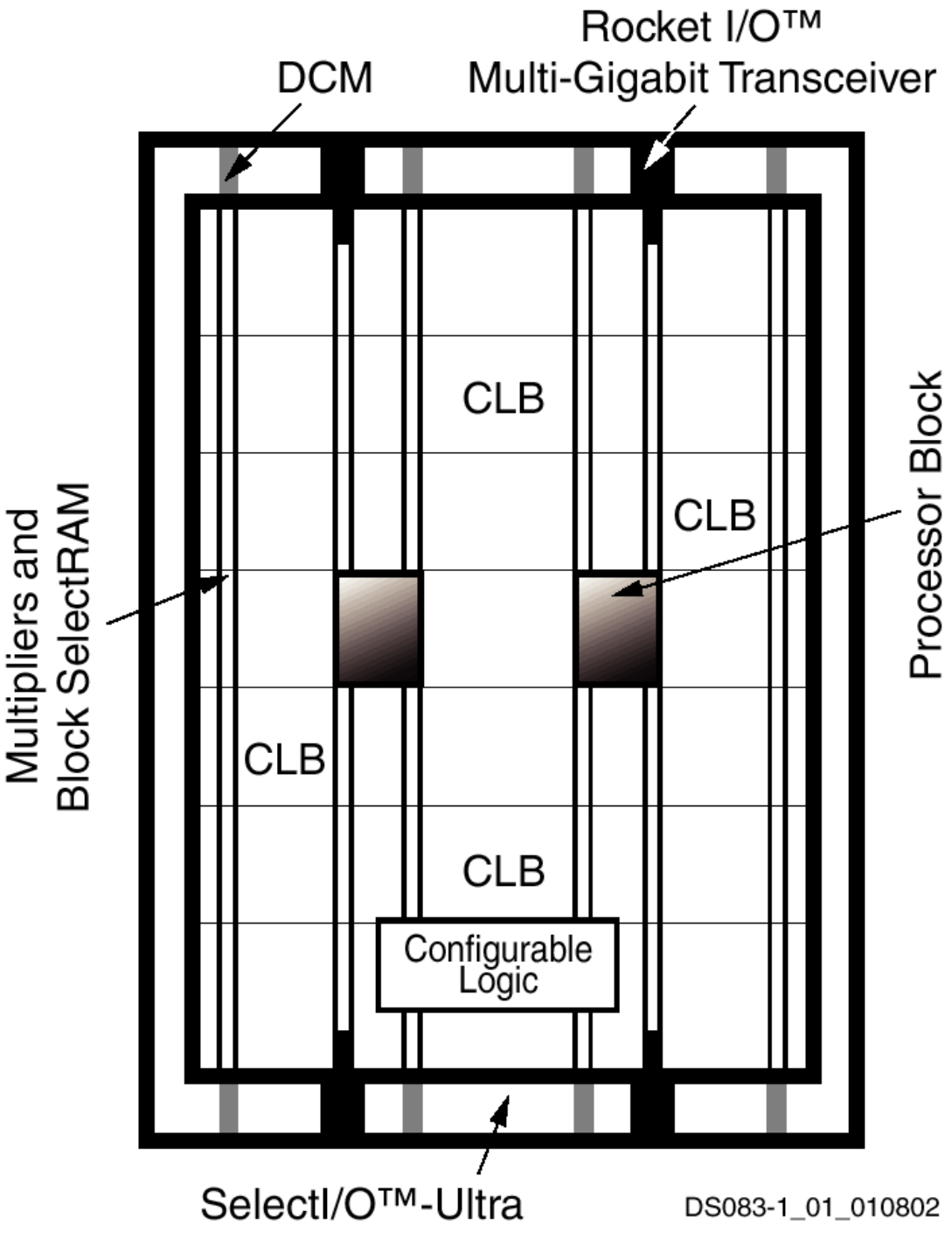
[© and source: Xilinx Inc.: Virtex-II Pro™ Platform FPGAs: Functional Description, Sept. 2002, //www.xilinx.com]

Interconnect

Hierarchical Routing Resources

24 Horizontal Long Lines 24 Vertical Long Lines	
120 Horizontal Hex Lines 120 Vertical Hex Lines	
40 Horizontal Double Lines 40 Vertical Double Lines	
16 Direct Connections (total in all four directions)	
8 Fast Connects	

Virtex II Pro Devices include up to 4 PowerPC processor cores



[© and source: Xilinx Inc.: Virtex-II Pro™ Platform FPGAs: Functional Description, Sept. 2002, //www.xilinx.com]

Memory

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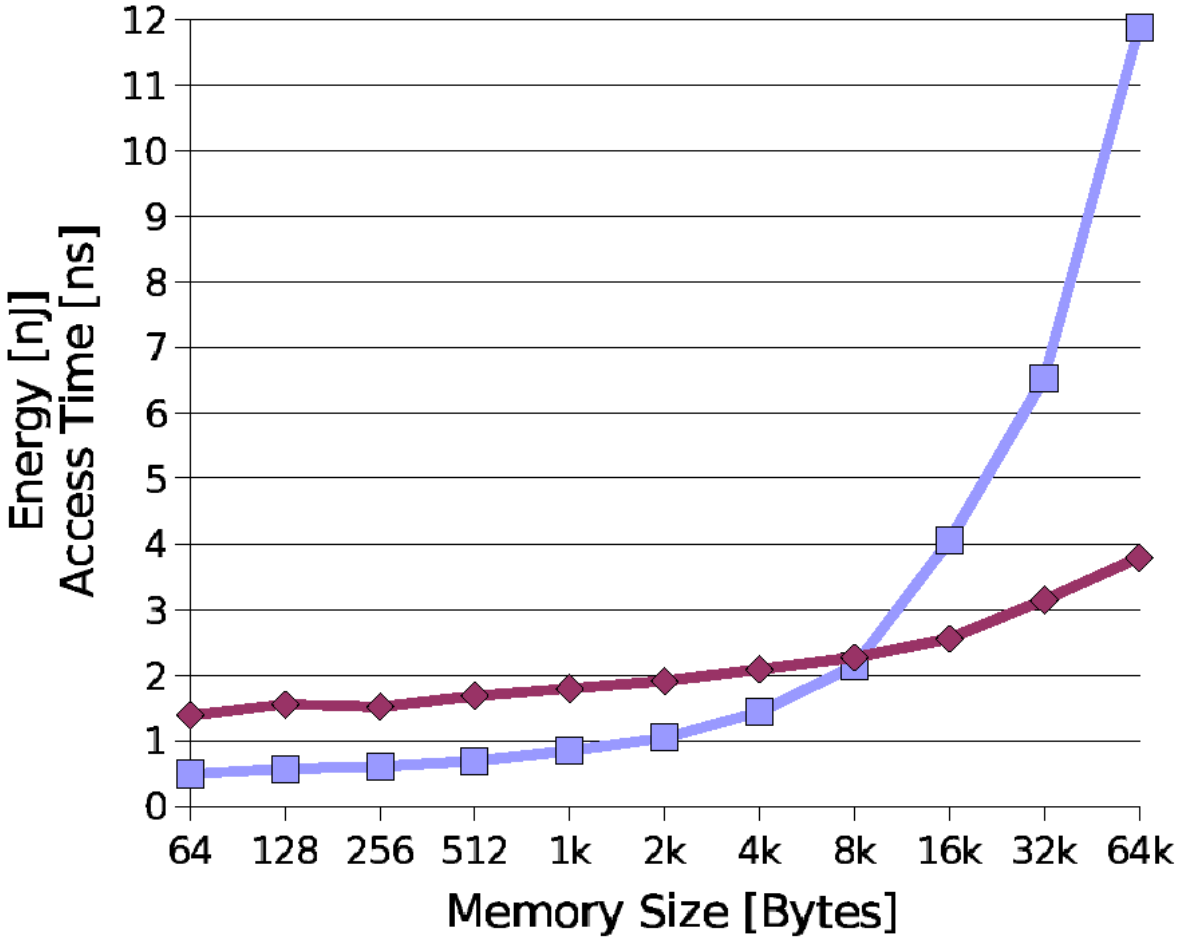
Memory

For the memory, efficiency is again a concern:

- speed (latency and throughput); predictable timing
- energy efficiency
- size
- cost
- other attributes (volatile vs. persistent, etc)

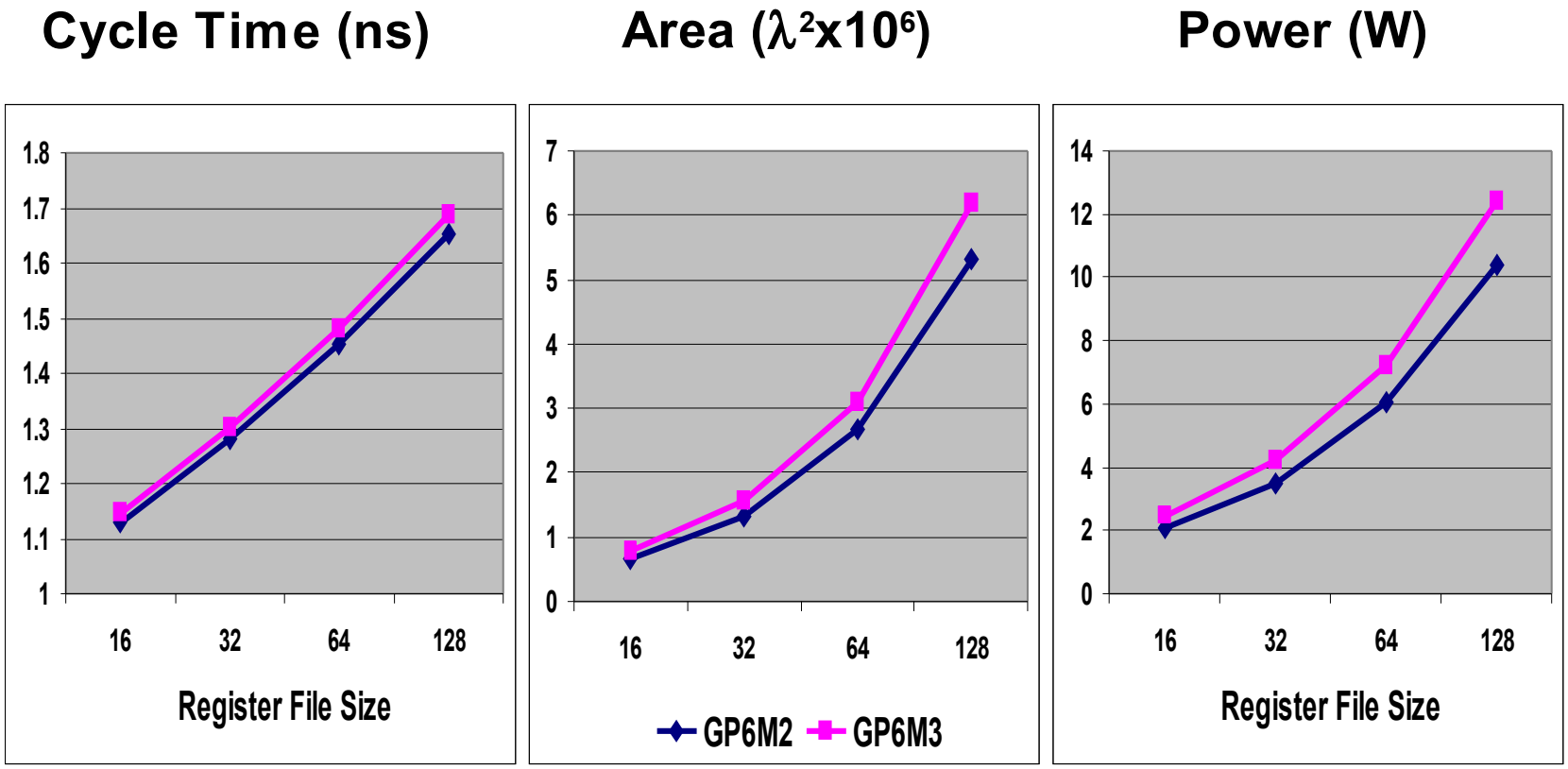
Access times and energy consumption increases with the size of the memory

Example (CACTI Model):



"Currently, the size of some applications is doubling every 10 months"
[STMicroelectronics, Medea+ Workshop, Stuttgart, Nov. 2003]

Access times and energy consumption for multi-ported register files

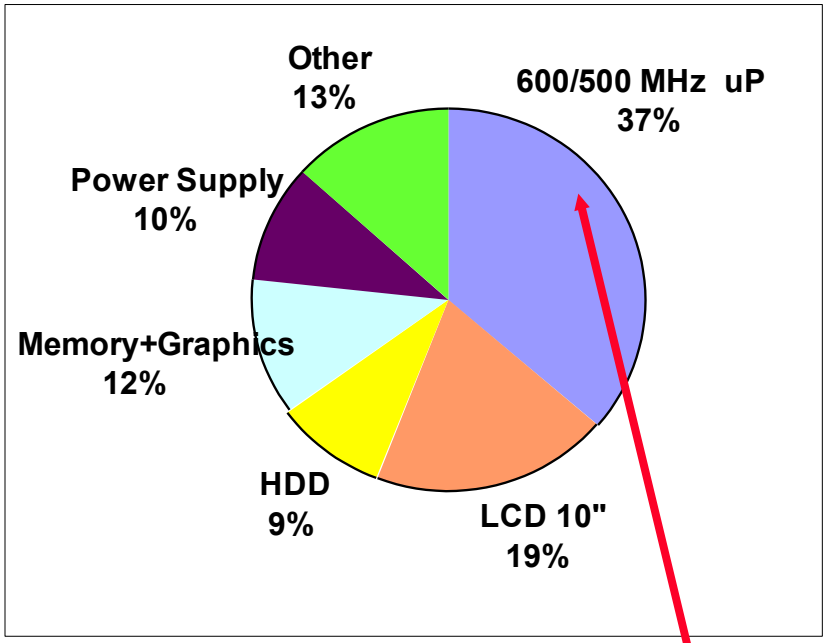


Rixner's et al. model [HPCA'00], Technology of 0.18 μm

Source and © H. Valero, 2001

How much of the energy consumption of a system is memory-related?

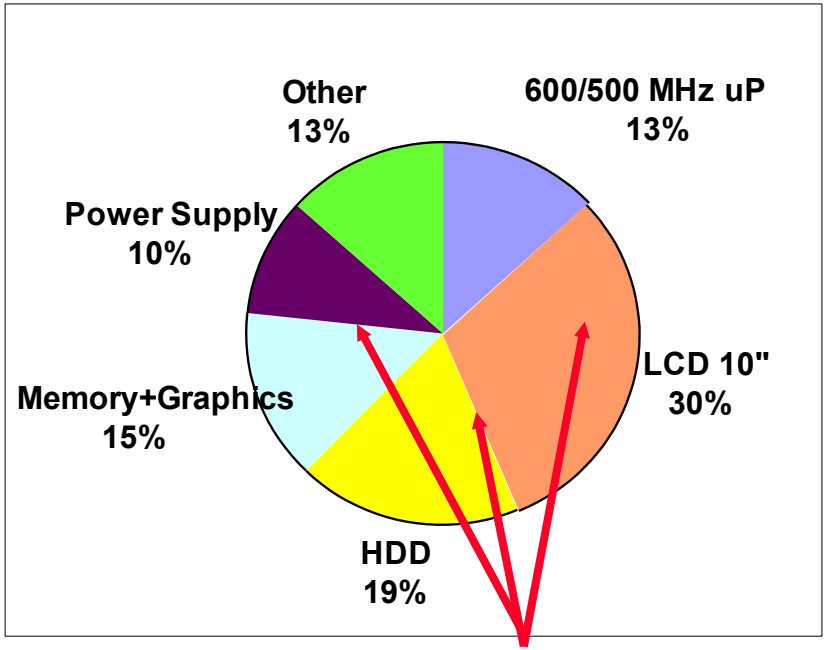
Mobile PC
Thermal Design (TDP) System Power



Note: Based on Actual Measurements

CPU Dominates Thermal Design Power

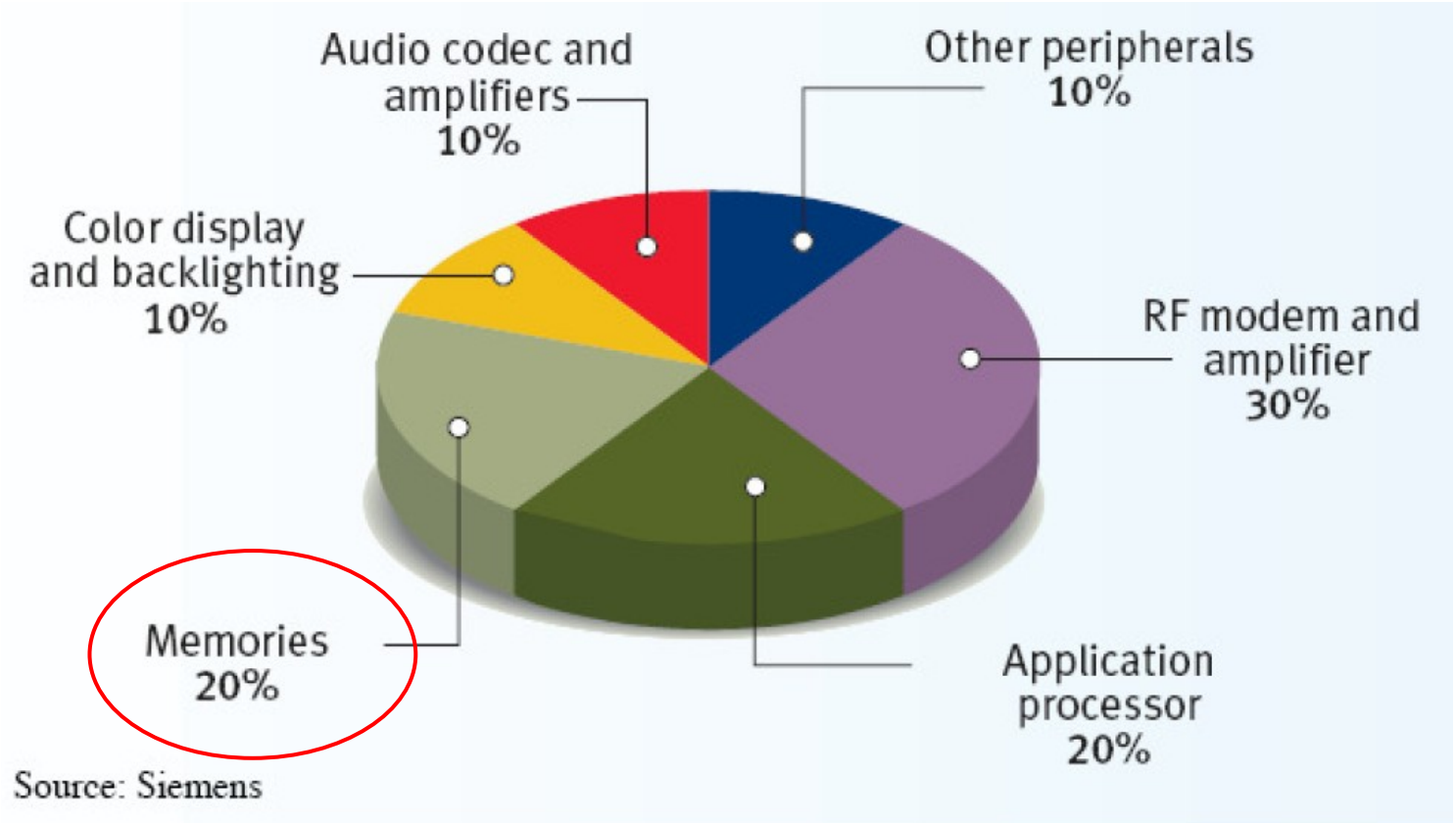
Mobile PC
Average System Power



Multiple Platform Components Comprise Average Power

[Courtesy: N. Dutt; Source: V. Tiwari]

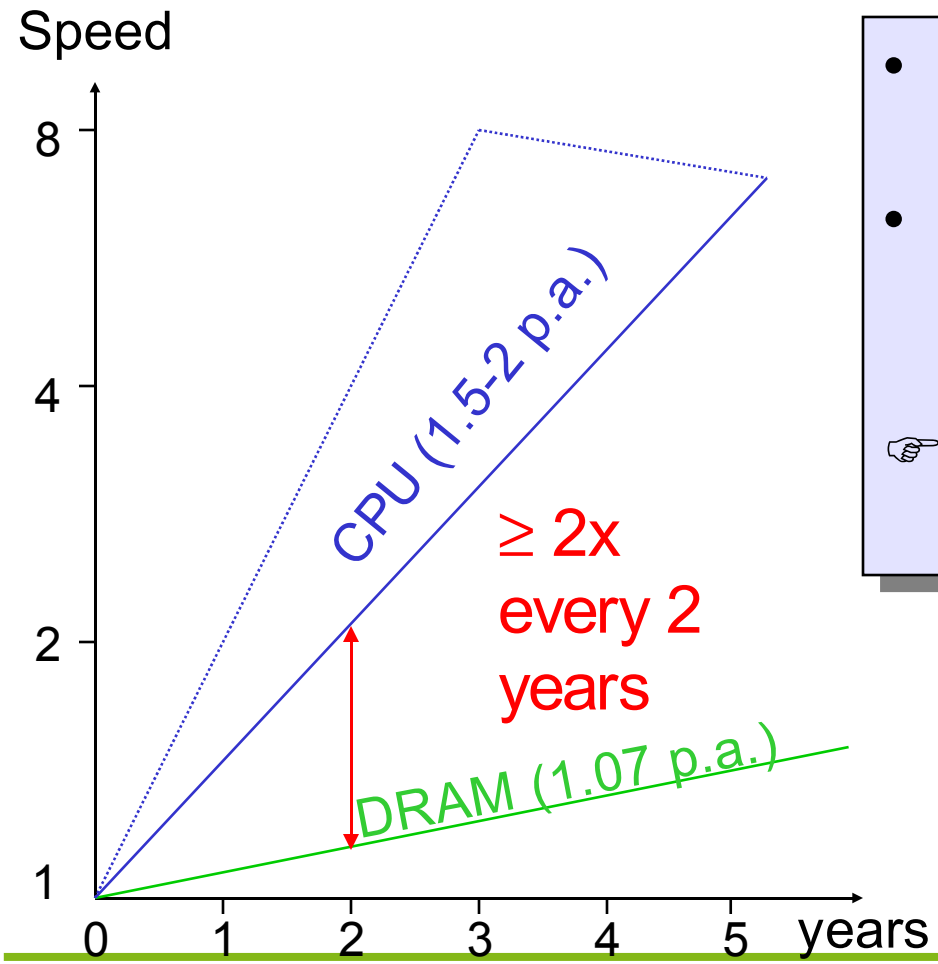
Energy consumption in mobile devices



[O. Vargas (Infineon Technologies): Minimum power consumption in mobile-phone memory subsystems; Pennwell Portable Design - September 2005;] Thanks to Thorsten Koch (Nokia/ Univ. Dortmund) for providing this source.

Access-times will be a problem

Speed gap between processor and main DRAM increases



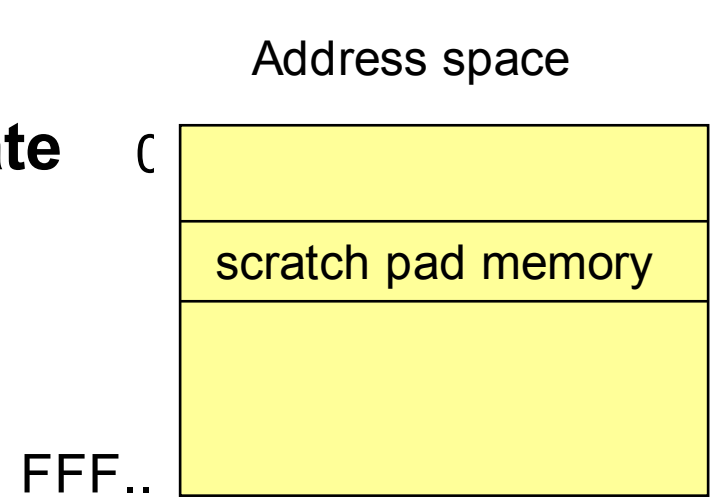
- early 60ties (Atlas): page fault ~ 2500 instructions
- 2002 (2 GHz µP): access to DRAM ~ 500 instructions

☞ penalty for cache miss about same as for page fault in Atlas

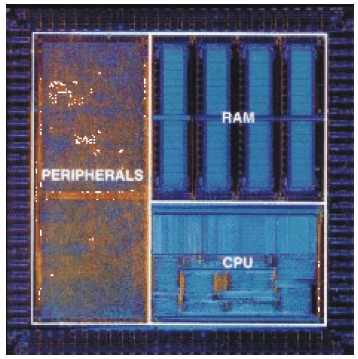
[P. Machanik: Approaches to Addressing the Memory Wall, TR Nov. 2002, U. Brisbane]

Hierarchical memories using scratch pad memories (SPM)

SPM is a small, physically separate memory mapped into the address space

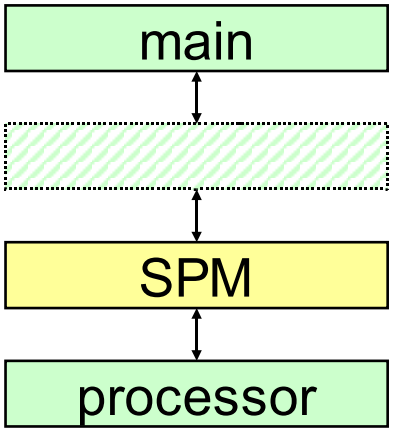


Example

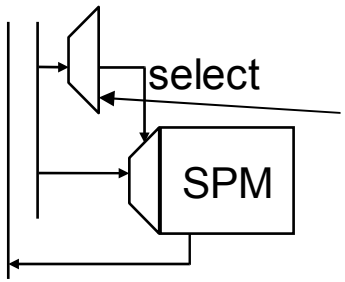


ARM7TDMI cores, well-known for low power consumption

Hierarchy



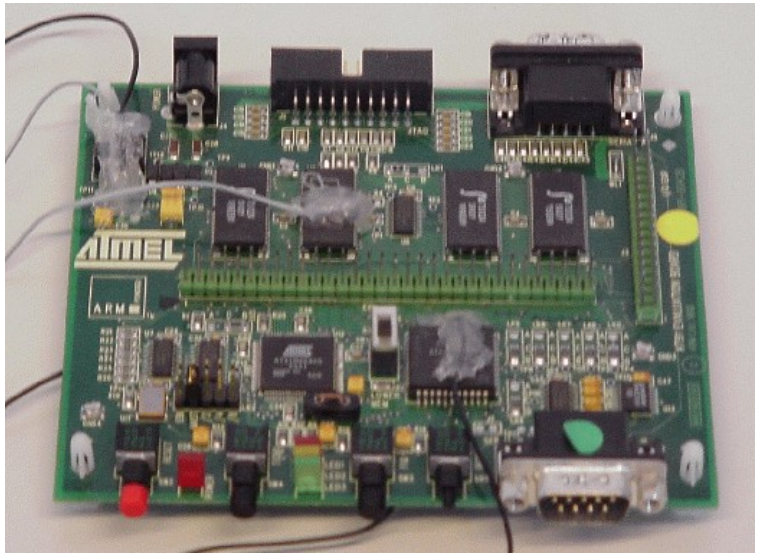
no tag memory

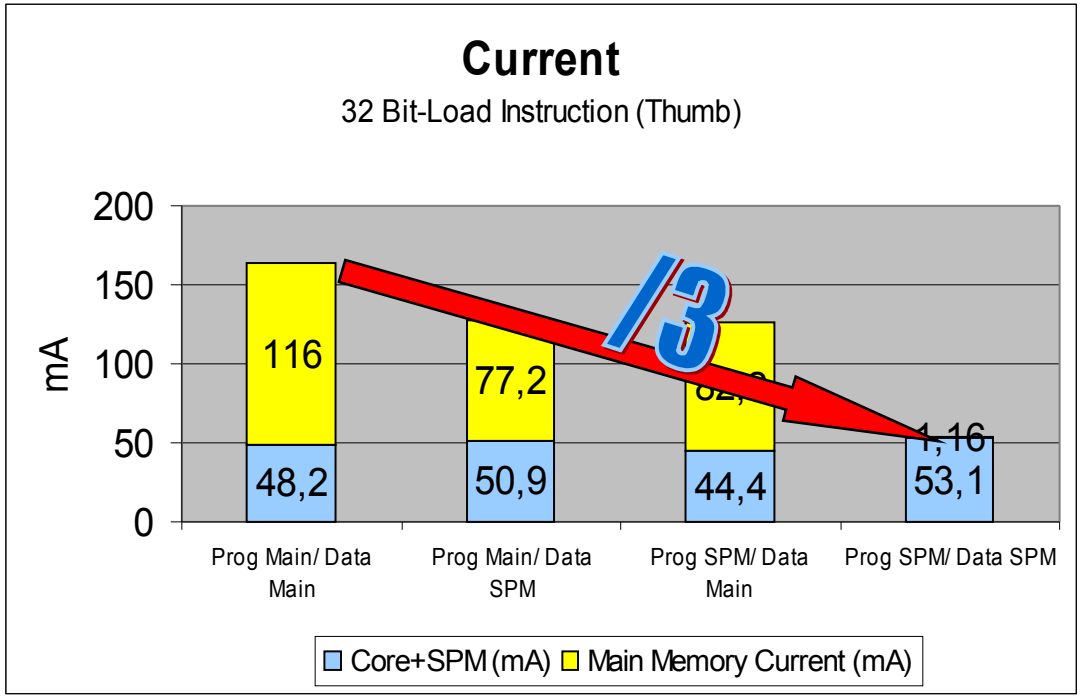


Selection is by an appropriate address decoder (simple!)

Comparison of currents using measurements

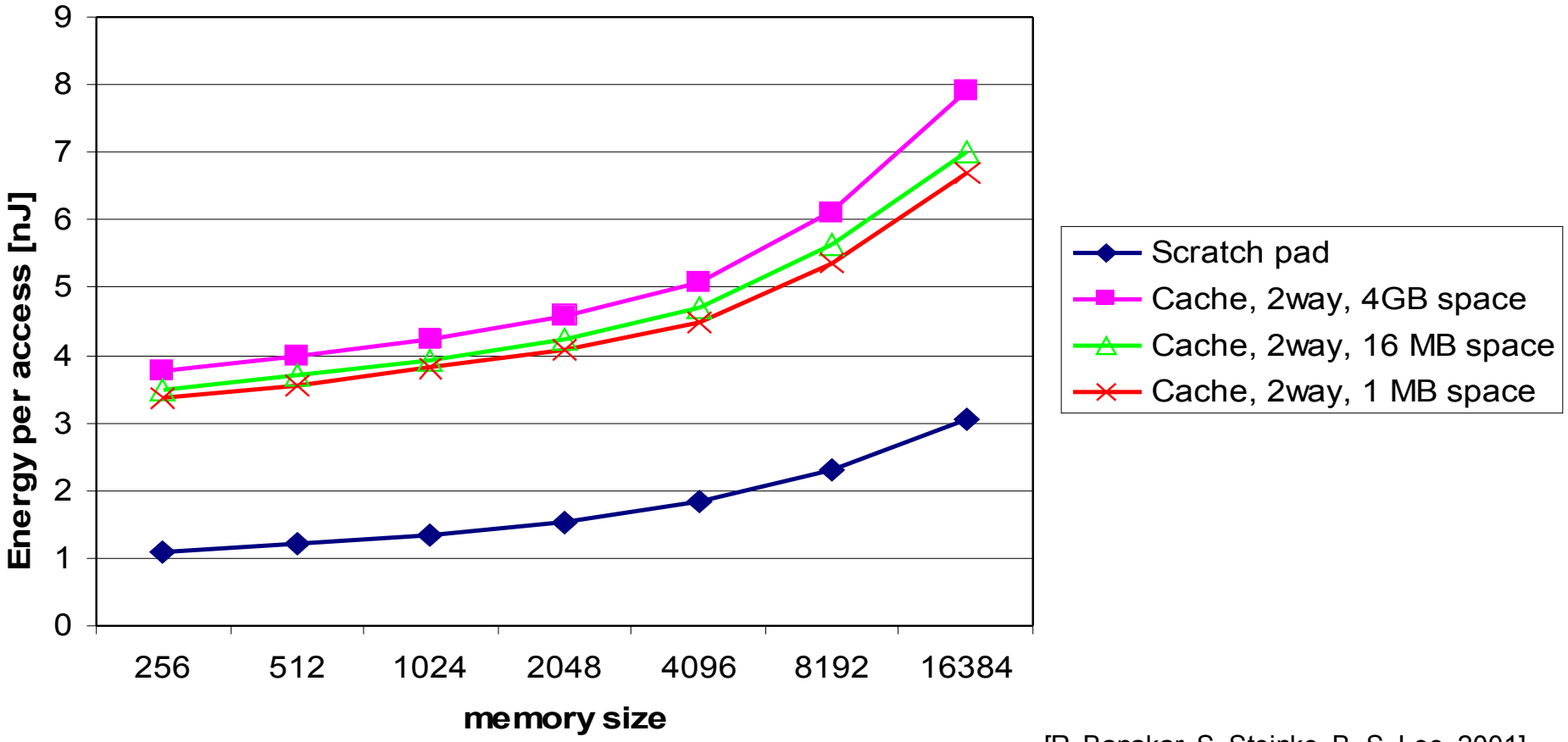
E.g.: ATMEL board with ARM7TDMI and ext. SRAM





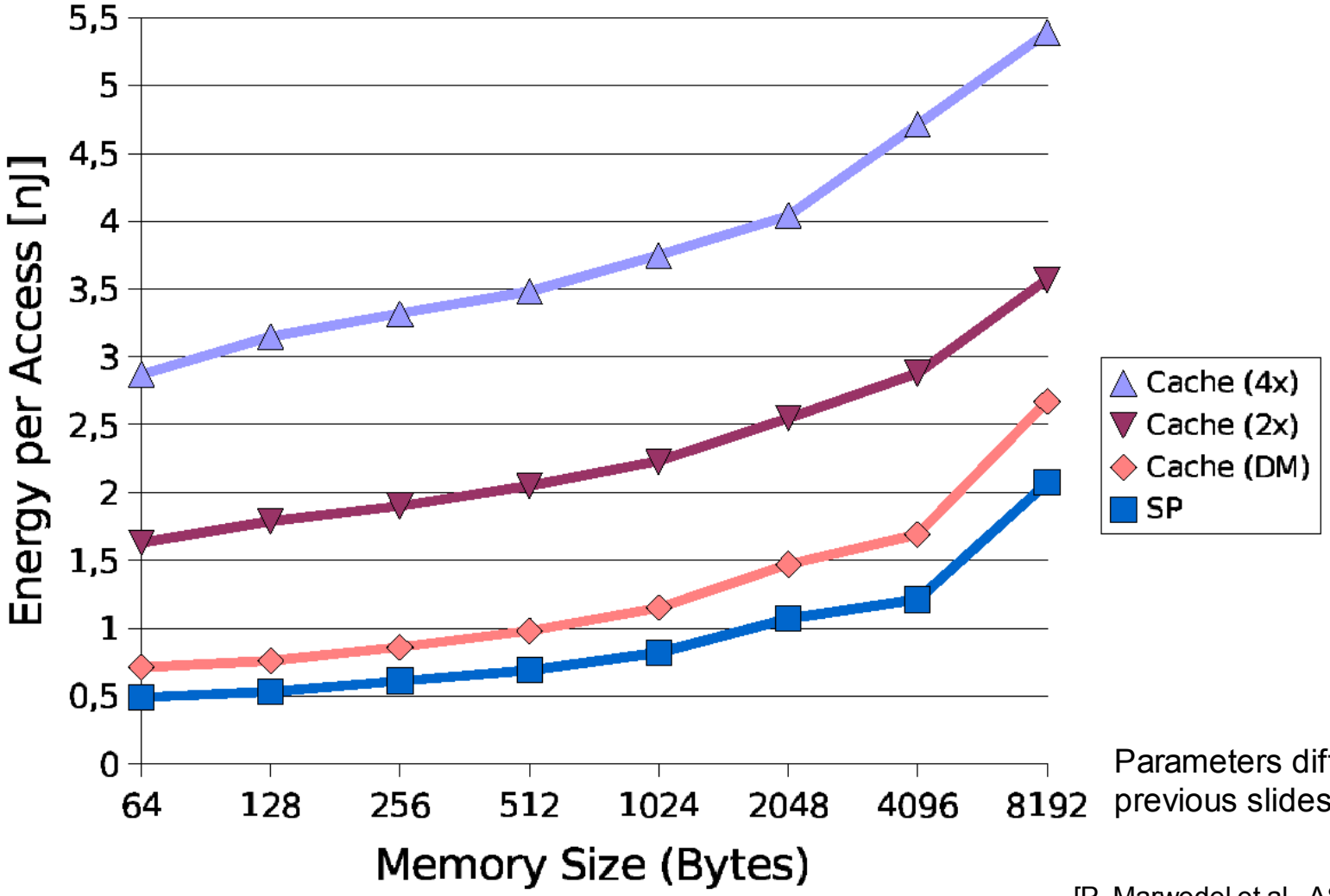
Why not just use a cache ? (1)

1. Energy for parallel access of sets, in comparators, muxes.



[R. Banakar, S. Steinke, B.-S. Lee, 2001]

Influence of the associativity



Parameters different from previous slides

[P. Marwedel et al., ASPDAC, 2004]

D/A-Converters

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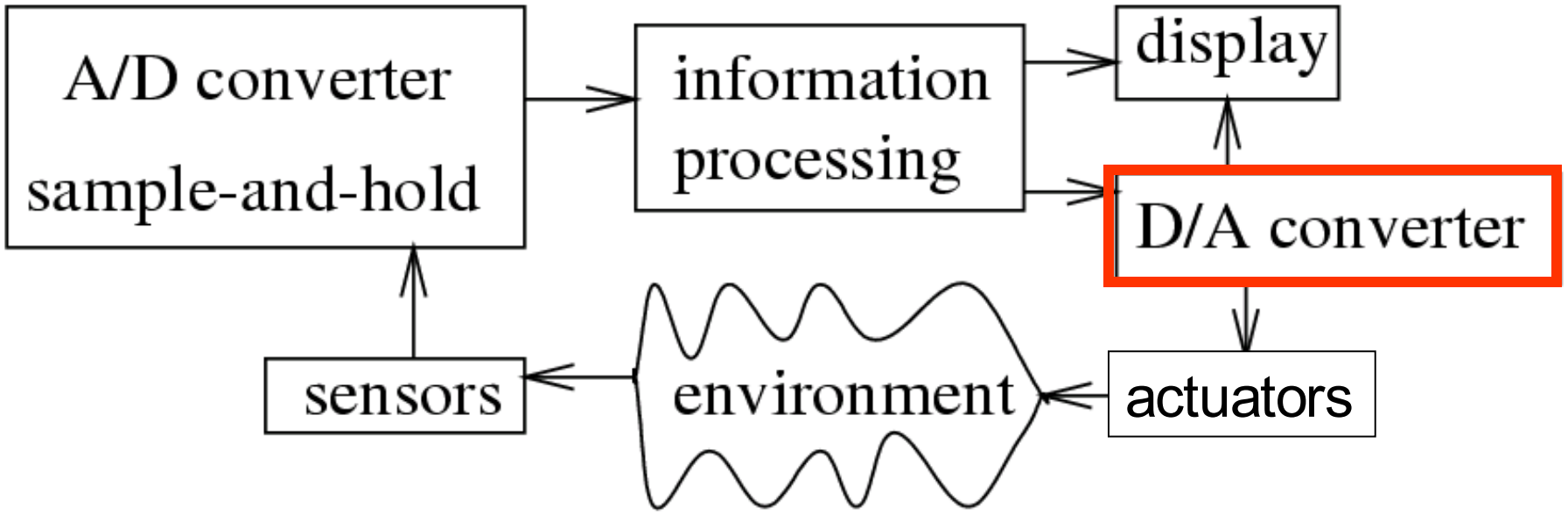
Embedded System Hardware

Embedded system hardware is frequently used in a loop (***„hardware in a loop“***):

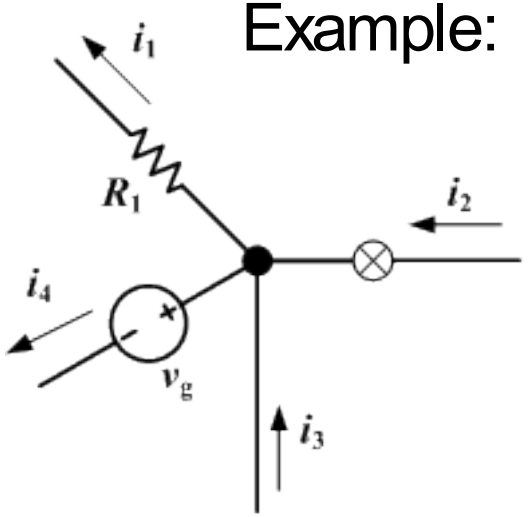


Kirchhoff's junction rule

Kirchhoff's Current Law, Kirchhoff's first rule

The principle of conservation of electric charge implies that:
At any point in an electrical circuit where charge density is not changing in time, the sum of currents flowing towards that point is equal to the sum of currents flowing away from that point.

Example:



www.wikipedia.org

$$i_1 + i_4 = i_2 + i_3$$

Formally, for any node in a circuit:

$$\sum_k i_k = 0$$

$$-i_1+i_2+i_3-i_4=0$$

Count current flowing away from node as negative.

Kirchhoff's loop rule

Kirchhoff's Voltage Law, Kirchhoff's second rule

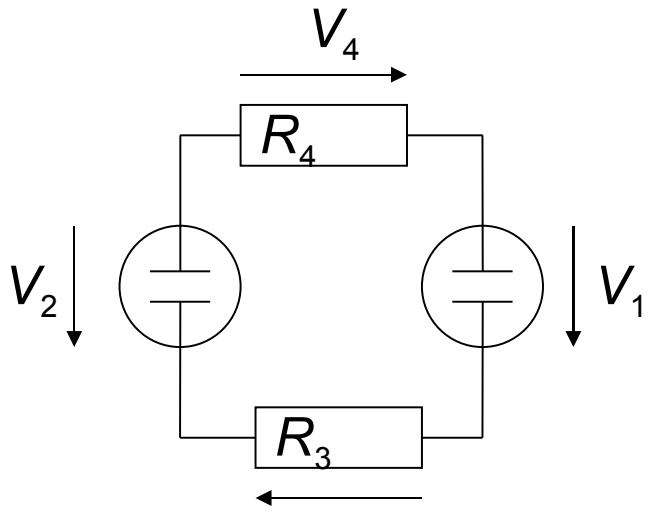
The principle of conservation of energy implies that:
The directed sum of the electrical potential differences around a closed circuit must be zero.
Otherwise, it would be possible to build a perpetual motion machine that passed a current in a circle around the circuit.
[www.wikipedia.org]

Formally, for any loop in a circuit:

$$\sum_k V_k = 0$$

Count voltages traversed against arrow direction as negative

Example:



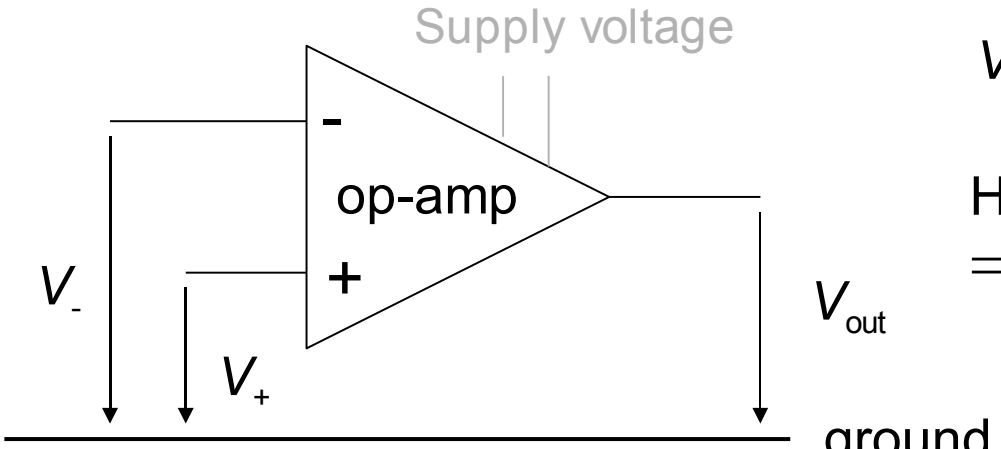
$V_1+V_3-V_2+V_4=0$

$V_3=R_3\times I$ if current counted in the same direction as V_3

$V_3=-R_3\times I$ if current counted in the opposite direction as V_3

Operational Amplifiers (Op-Amps)

Operational amplifiers (op-amps) are devices amplifying the voltage difference between two input terminals by a large gain factor *g*



$$V_{out}=(V_+ - V_-) \cdot g$$

High impedance input terminals
$\Rightarrow$ Currents into inputs ≈ 0

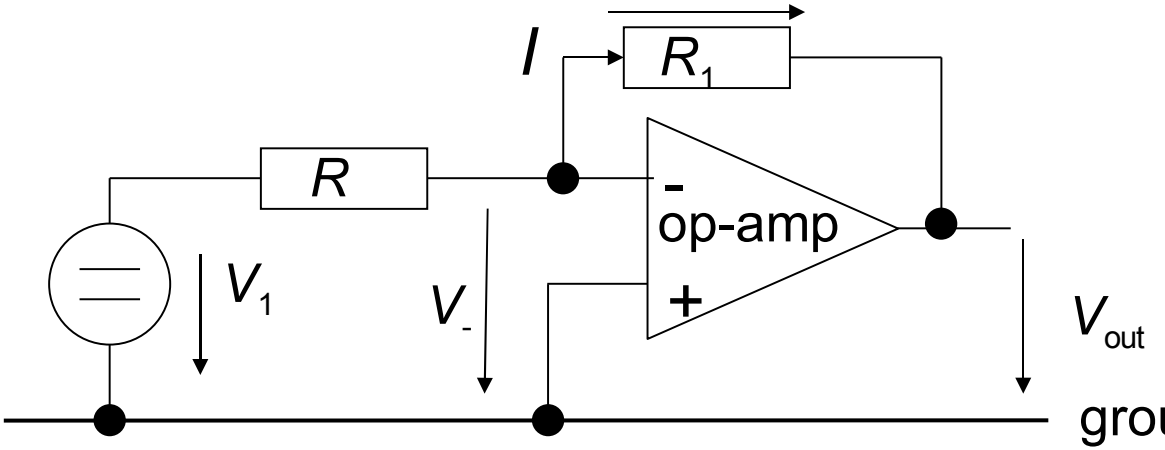
Op-amp in a separate package (TO-5) [wikipedia]

For an **ideal** op-amp: $g \rightarrow \infty$

(In practice: *g* may be around $10^4..10^6$)

Op-Amps with feedback

In circuits, negative feedback is used to define the actual gain



Due to the feedback to the *inverted* input, R_1 reduces voltage V_-. To which level?

$V_{out} = - g \cdot V_-$ (op-amp feature)

$I \cdot R_1 + V_{out} - V_- = 0$ (loop rule)

$\Rightarrow I \cdot R_1 + - g \cdot V_- - V_- = 0$

$\Rightarrow (1+g) \cdot V_- = I \cdot R_1$

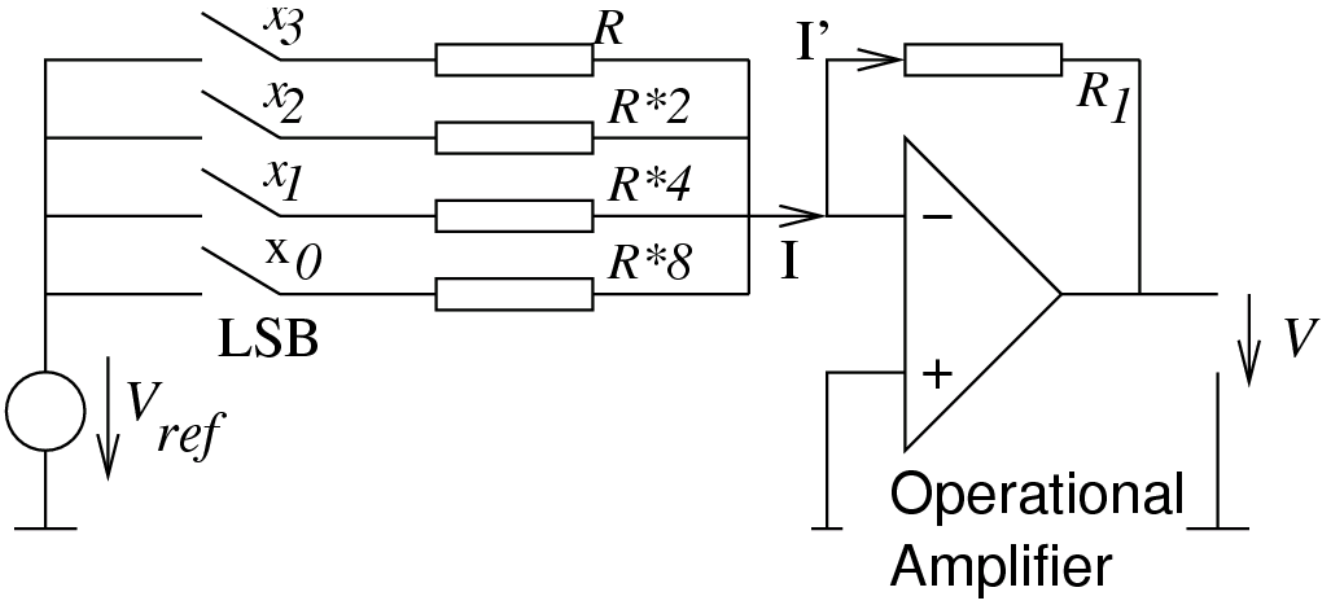
$$\Rightarrow V_- = \frac{I \cdot R_1}{1+g}$$

$$V_{-,ideal} = \lim_{g \to \infty} \frac{I \cdot R_1}{1+g} = 0$$

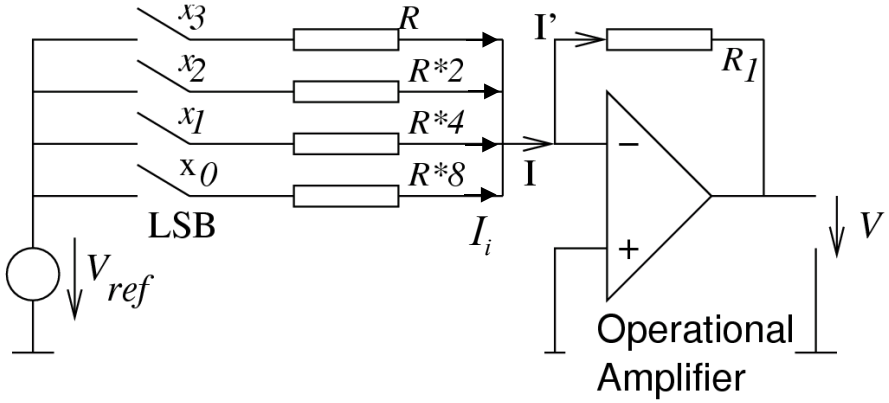
V_- is called **virtual ground**: the voltage is 0, but the terminal may not be connected to ground

Digital-to-Analog (D/A) Converters

Various types, can be quite simple,
e.g.:



Output voltage ~ no. represented by x



Loop rule: $I_i = x_i \times \frac{V_{ref}}{2^{3-i} \times R}$ $\quad I = \sum_i I_i$

☞ $I = x_3 \times \frac{V_{ref}}{R} + x_2 \times \frac{V_{ref}}{2 \times R} + x_1 \times \frac{V_{ref}}{4 \times R} + x_0 \times \frac{V_{ref}}{8 \times R}$

$= \frac{V_{ref}}{R} \times \sum_{i=0}^{3} x_i \times 2^{i-3}$

Loop rule: $V + R_1 \times I' = 0$

Junction rule: $I = I'$

Hence: $V + R_1 \times I = 0$

Finally: $-V = V_{ref} \times \frac{R_1}{R} \sum_{i=0}^{3} x_i \times 2^{i-3} = V_{ref} \times \frac{R_1}{8 \times R} \times nat(x)$

$I \sim nat\,(x)$, where $nat(x)$:
natural number represented by x;
Op-amp turns this current into a voltage $\sim nat\,(x)$

Output

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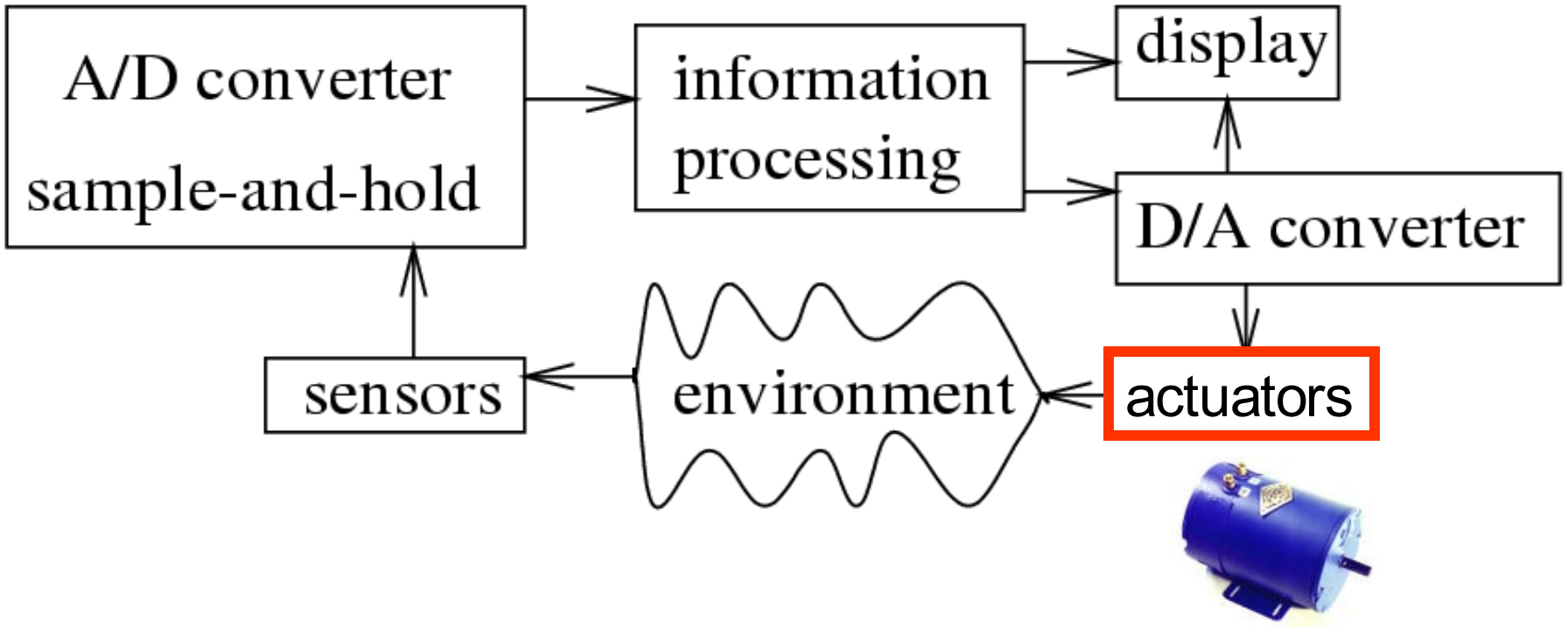
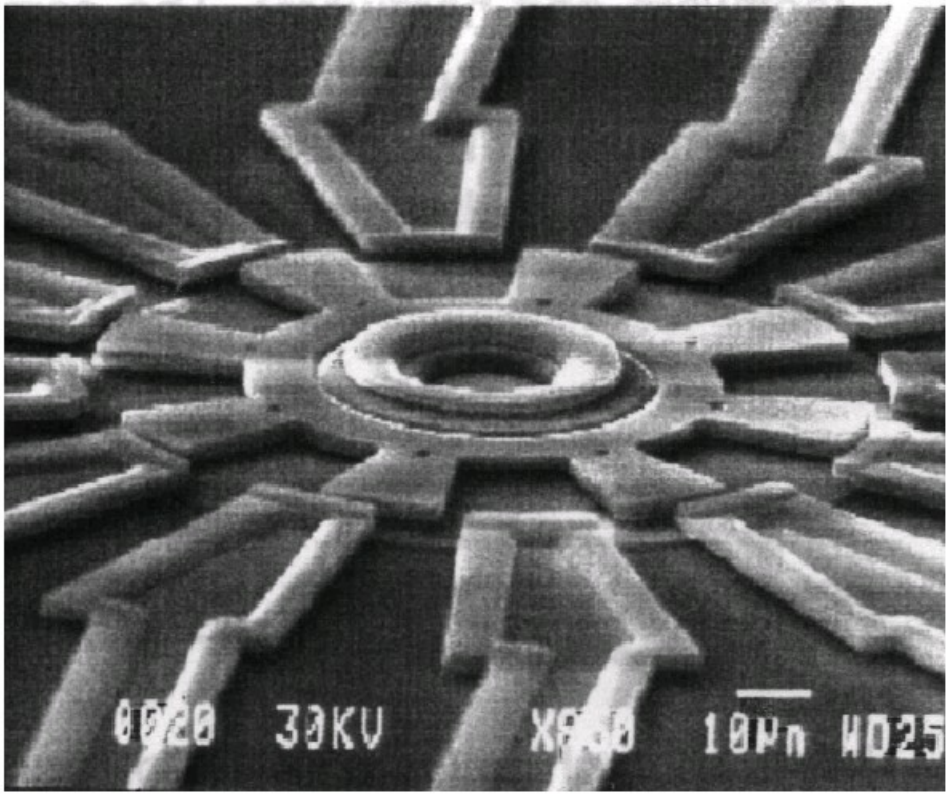


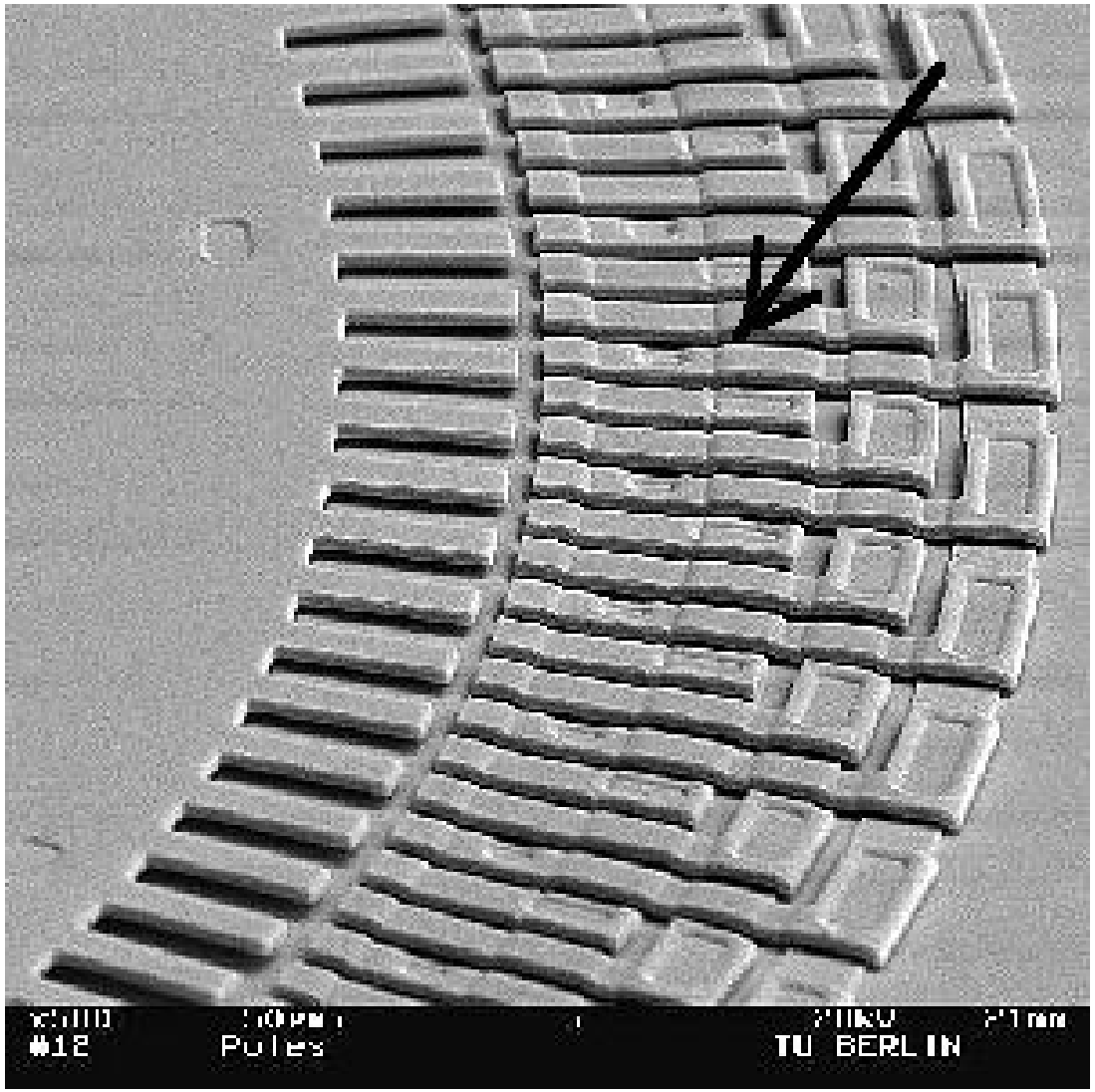
Actuators and output

Huge variety of actuators and output devices, impossible to present all of them.
Microsystems motors as examples (© MCNC):



(© MCNC)

Actuators and output (2)



Courtesy and ©:
E. Obermeier, MAT,
TU Berlin

Summary

Hardware in a loop

- Sensors
- Discretization
- Information processing
  - Importance of energy efficiency
  - Special purpose HW very expensive
  - Energy efficiency of processors
  - Code size efficiency
  - Run-time efficiency
  - Reconfigurable Hardware
- D/A converters
- Actuators