FPGA-Programming

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Informatik 12, U. Dortmund
Importance of Energy Efficiency

- **IPE** = Inherent power efficiency
- **AmI** = Ambient Intelligence

![Graph showing the importance of energy efficiency over time, with 32-bit systems indicated and noting the lack of V_{DD} scaling.]

Stuck at 200Gop/J

Courtesy: Philips © Hugo De Man, IMEC, 2007
Challenges for implementation in hardware

- Lack of flexibility (changing standards).
- Mask cost for specialized HW becomes very expensive.

Special hardware is ruled out for many applications, but energy efficiency is still required.

Reconfigurable Logic

Full custom chips may be too expensive, software too slow.

- Combine the speed of HW with the flexibility of SW
- HW with programmable functions and interconnect.
- Use of configurable hardware;
  common form: field programmable gate arrays (FPGAs)

Applications: bit-oriented algorithms like

- encryption,
- fast „object recognition“ (medical and military),
- Adapting mobile phones to different standards.

Very popular devices from

- XILINX (e.g. XILINX Vertex II)
- Actel and others
Gliederung

- Einführung
- SystemC
  - Vorlesungen und Programmierung
- FPGAs
  - Vorlesungen
  - VHDL-basierte Konfiguration von FPGAs mit dem XUP VII Pro Entwicklungssystem
- Algorithmen
  - Mikroarchitektur-Synthese
  - Automatensynthese
  - Logiksynthese
  - Layoutsynthese

Zeitplan

3,5 Wochen
3,5 Wochen
6 Wochen
Xilinx University Program (XUP)
Virtex II Pro Development Board

We are using a large board of the XUP line.

http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?iLanguageID=1&category=-1212168&sGlobalNavPick=&sSecondaryNavPick=
The board includes a good number of I/O interfaces.

- External Power
- Internal Power Supplies: 3.3V, 2.5V, 1.5V
- CPU Debug Port
- 100 MHz System Clock
- 75 MHz SATA Clock
- User Clocks (2)
- Platform Flash Configurations (2)
- Compact Flash Configurations (8)
- USB2 High Speed Configuration
- AC97 Audio CODEC & Stereo Amp
- XSGA Video Output
- User LEDs (4)
- User Switches (4)
- User Push-button Switches (5)
- 10/100 Ethernet PHY
- RS-232 & PS/2 Ports (2)
- Serial ATA Ports (3)
- Multi-Gigabit Transceiver Port
- 2 GB DDR SDRAM DIMM Module
- 5V Tolerant Expansion Headers
- High Speed Expansion Port
Properties of the Virtex™-II Pro board (1)

- Virtex™-II Pro FPGA with PowerPC™ 405 cores
- Up to 2 GB of Double Data Rate (DDR) SDRAM
- System ACE™ controller and Type II CompactFlash™ connector for FPGA configuration and data storage
- Embedded Platform Cable USB configuration port
- High-speed SelectMAP FPGA configuration from Platform Flash In-System
- Programmable Configuration PROM
- Support for “Golden” and “User” FPGA configuration bitstreams
- On-board 10/100 Ethernet PHY device
- Silicon Serial Number for unique board identification
- RS-232 DB9 serial port
- Two PS-2 serial ports
- Four LEDs connected to Virtex-II Pro I/O pins
- Four switches connected to Virtex-II Pro I/O pins
- Five push buttons connected to Virtex-II Pro I/O pins
Properties of the Virtex™-II Pro board (2)

- Six expansion connectors joined to 80 Virtex-II Pro I/O pins with over-voltage protection
- High-speed expansion connector joined to 40 Virtex-II Pro I/O pins that can be used differentially or single ended
- AC-97 audio CODEC with audio amplifier and speaker/headphone output and line level output
- Microphone and line level audio input
- On-board XSGA output, up to 1200 x 1600 at 70 Hz refresh
- Three Serial ATA ports, two Host ports and one Target port
- Off-board expansion MGT link, with user-supplied clock
- 100 MHz system clock, 75 MHz SATA clock
- Provision for user-supplied clock
- On-board power supplies
- Power-on reset circuitry
- PowerPC 405 reset circuitry
# User LED and switch connections

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>FPGA Pin</th>
<th>I/O Type</th>
<th>Drive</th>
<th>Slew</th>
</tr>
</thead>
<tbody>
<tr>
<td>LED_0</td>
<td>O</td>
<td>AC4</td>
<td>LVTTL</td>
<td>12 mA</td>
<td>SLOW</td>
</tr>
<tr>
<td>LED_1</td>
<td>O</td>
<td>AC3</td>
<td>LVTTL</td>
<td>12 mA</td>
<td>SLOW</td>
</tr>
<tr>
<td>LED_2</td>
<td>O</td>
<td>AA6</td>
<td>LVTTL</td>
<td>12 mA</td>
<td>SLOW</td>
</tr>
<tr>
<td>LED_3</td>
<td>O</td>
<td>AA5</td>
<td>LVTTL</td>
<td>12 mA</td>
<td>SLOW</td>
</tr>
<tr>
<td>SW_0</td>
<td>I</td>
<td>AC11</td>
<td>LVCMOS25</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>SW_1</td>
<td>I</td>
<td>AD11</td>
<td>LVCMOS25</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>SW_2</td>
<td>I</td>
<td>AF8</td>
<td>LVCMOS25</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>SW_3</td>
<td>I</td>
<td>AF9</td>
<td>LVCMOS25</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>PB_ENTER</td>
<td>I</td>
<td>AG5</td>
<td>LVTTL</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>PB_UP</td>
<td>I</td>
<td>AH4</td>
<td>LVTTL</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>PB_DOWN</td>
<td>I</td>
<td>AG3</td>
<td>LVTTL</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>PB_LEFT</td>
<td>I</td>
<td>AH1</td>
<td>LVTTL</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>PB_RIGHT</td>
<td>I</td>
<td>AH2</td>
<td>LVTTL</td>
<td>–</td>
<td>–</td>
</tr>
</tbody>
</table>
Configuration data path

Very flexible set of configuration options.
Selecting the proper initialization (1)

(Power up) or (RESET_RELOAD (SW1) pressed for >2 s): FPGA begins configuring 2 configuration methods, selected by CONFIG SOURCE switch (MSB (left) of SW9):

- If CONFIG SOURCE switch is closed, or up: high-speed SelectMap byte-wide configuration from on-board Platform Flash configuration PROM (U3) is selected, PROM CONFIG LED (D19) on.
  
PROM supports 2 configs., selected by PROM VERSION switch = LSB of SW9.
  - PROM VERSION switch is closed, or up:
    GOLDEN config. from onboard Platform Flash configuration PROM selected, GOLDEN CONFIG LED (D14) = on.
    Config. can be board test utility provided by Xilinx. 
    PROM VERSION switch sampled only at powerup and system reset.
    If switch changed later: RESET_RELOAD must be pressed for > 2 seconds.
  - PROM VERSION switch is open, or down: User configuration from the on-board Platform Flash configuration PROM is selected. This configuration must be programmed into the Platform Flash PROM from the JTAG Platform Cable USB interface or the USB interface following the instructions in Appendix B.

Platform Flash is normally disabled after configuring (DONE='1').
If additional data to be read, jumper JP9 must be moved to EXTENDED.
FPGA Start-Up Clock should be set to CCLK in the Startup Options section of the Process Options for the generation of the programming file.
Selecting the proper initialization (2)

- If CONFIG SOURCE switch is *open*, *off*, or *down*, a lower speed JTAG-based configuration from Compact Flash or external JTAG source is selected, JTAG CONFIG LED (D20)=on.

  - Default source is from the Compact Flash port (J7). If configuration data exists on the CF card, it becomes the source for the configuration data. The CF card supports up to eight different configuration data files, selected by the triple CF CONFIG SELECT DIP switch (SW8). During configuration, SYSTEMACE STATUS LED (D12) flashes. At completion: FPGA asserts the FPGA_DONE signal, DONE LED (D4) on. Any time: RESET_RELOAD on for >2 s: one of 8 configuration files loaded. D11 flashes if no *valid* configuration file is found on the Compact Flash card.

  - The high-speed embedded Platform Cable USB configuration port (J8) is enabled if no configuration is found on the CF card.

JTAG Clock should be selected in the Startup Options section of the Process Options for the generation of the programming file.
### Number of resources available in Virtex II Pro devices

#### Table 16: Virtex-II Pro Logic Resources Available in All CLBs

<table>
<thead>
<tr>
<th>Device</th>
<th>CLB Array: Row x Column</th>
<th>Number of Slices</th>
<th>Number of LUTs</th>
<th>Max Distributed SelectRAM+ or Shift Register (bits)</th>
<th>Number of Flip-Flops</th>
<th>Number of Carry Chains(1)</th>
<th>Number of SOP Chains(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC2VP2</td>
<td>16 x 22</td>
<td>1,408</td>
<td>2,816</td>
<td>45,056</td>
<td>2,816</td>
<td>44</td>
<td>32</td>
</tr>
<tr>
<td>XC2VP4</td>
<td>40 x 22</td>
<td>3,008</td>
<td>6,016</td>
<td>96,256</td>
<td>6,016</td>
<td>44</td>
<td>80</td>
</tr>
<tr>
<td>XC2VP7</td>
<td>40 x 34</td>
<td>4,928</td>
<td>9,856</td>
<td>157,696</td>
<td>9,856</td>
<td>68</td>
<td>80</td>
</tr>
<tr>
<td>XC2VP20</td>
<td>56 x 46</td>
<td>9,280</td>
<td>18,560</td>
<td>296,960</td>
<td>18,560</td>
<td>92</td>
<td>112</td>
</tr>
<tr>
<td><strong>XC2VP30</strong></td>
<td><strong>80 x 46</strong></td>
<td><strong>13,696</strong></td>
<td><strong>27,392</strong></td>
<td><strong>438,272</strong></td>
<td><strong>27,392</strong></td>
<td><strong>92</strong></td>
<td><strong>160</strong></td>
</tr>
<tr>
<td>XC2VP40</td>
<td>88 x 58</td>
<td>19,392</td>
<td>38,784</td>
<td>620,544</td>
<td>38,784</td>
<td>116</td>
<td>176</td>
</tr>
<tr>
<td>XC2VP50</td>
<td>88 x 70</td>
<td>23,616</td>
<td>47,232</td>
<td>755,712</td>
<td>47,232</td>
<td>140</td>
<td>176</td>
</tr>
<tr>
<td>XC2VP70</td>
<td>104 x 82</td>
<td>33,088</td>
<td>66,176</td>
<td>1,058,816</td>
<td>66,176</td>
<td>164</td>
<td>208</td>
</tr>
<tr>
<td>XC2VP100</td>
<td>120 x 94</td>
<td>44,096</td>
<td>88,192</td>
<td>1,411,072</td>
<td>88,192</td>
<td>188</td>
<td>240</td>
</tr>
<tr>
<td>XC2VP125</td>
<td>136 x 106</td>
<td>55,616</td>
<td>111,232</td>
<td>1,779,712</td>
<td>111,232</td>
<td>212</td>
<td>272</td>
</tr>
</tbody>
</table>

**Notes:**
1. The carry-chains and SOP chains can be split or cascaded.

Floor-plan of VIRTEX II FPGAs

Digital clock manager
I/O Blocks

Configurable Logic
Programmable I/Os

Block RAM
Multiplier
Virtex II Configurable Logic Block (CLB)

```
fast connects to neighbours
```

```
slice X1Y1
```

```
slice X1Y0
```

```
slice X0Y1
```

```
slice X0Y0
```

```
switch matrix
```

```
COUT
```

```
CIN
```

Look-up tables LUT F and G can be used to compute any Boolean function of ≤ 4 variables.
(½ of) Virtex II (Pro) Slice

[Diagram of Virtex II (Pro) Slice]

2 carry paths per CLB (Vertex II Pro)

Enables efficient implementation of adders.

Embedded Multipliers

A Virtex-II Pro multiplier block is an 18-bit by 18- signed multiplier.

Multipliers are connected to a switch matrix, share some bits with RAM (MAC instruction).

<table>
<thead>
<tr>
<th>Device</th>
<th>Columns</th>
<th>Multipliers</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC2VP2</td>
<td>4</td>
<td>12</td>
</tr>
<tr>
<td>XC2VP4</td>
<td>4</td>
<td>28</td>
</tr>
<tr>
<td>XC2VP7</td>
<td>6</td>
<td>44</td>
</tr>
<tr>
<td>XC2VP20</td>
<td>8</td>
<td>88</td>
</tr>
<tr>
<td>XC2VP30</td>
<td>8</td>
<td>136</td>
</tr>
<tr>
<td>XC2VPX20</td>
<td>8</td>
<td>88</td>
</tr>
<tr>
<td>XC2VP40</td>
<td>10</td>
<td>192</td>
</tr>
<tr>
<td>XC2VP50</td>
<td>12</td>
<td>232</td>
</tr>
<tr>
<td>XC2VP70</td>
<td>14</td>
<td>328</td>
</tr>
<tr>
<td>XC2VPX70</td>
<td>14</td>
<td>308</td>
</tr>
<tr>
<td>XC2VP100</td>
<td>16</td>
<td>444</td>
</tr>
</tbody>
</table>
Shift register configuration

Slices can be configured as shift registers
Implementing sums of products

Dedicated or chain for computing sum of products

16-input AND gate

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# Interconnect

<table>
<thead>
<tr>
<th>Hierarchical Routing Resources</th>
<th>Diagram</th>
</tr>
</thead>
<tbody>
<tr>
<td>24 Horizontal Long Lines</td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
</tr>
<tr>
<td>24 Vertical Long Lines</td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
</tr>
<tr>
<td>120 Horizontal Hex Lines</td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
</tr>
<tr>
<td>120 Vertical Hex Lines</td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
</tr>
<tr>
<td>40 Horizontal Double Lines</td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
</tr>
<tr>
<td>40 Vertical Double Lines</td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
</tr>
<tr>
<td>16 Direct Connections</td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
</tr>
<tr>
<td>(total in all four directions)</td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
</tr>
<tr>
<td>8 Fast Connects</td>
<td><img src="https://via.placeholder.com/150" alt="Diagram" /></td>
</tr>
</tbody>
</table>
3-state buffers

Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row.
Clock distribution

Up to 16 global clocks are available. 
≤ 8 clocks/quadrant can be used, organized in clock rows.
Virtex II Pro Devices include up to 4 PowerPC processor cores
Memory for processor cores

Cores are connected to local block RAM that can be used as a scratchpad.
Integrated PowerPC Processor

OCM=on chip memory controller; interface to Block SelectRAM+ serving as scratch pad memory

PLB=Processor local bus

MMU

Fetch & Decode

Fetch and Decode Logic

3-Element Fetch Queue
(PFB1, PFB0, DCD)

Execution Unit (EXU)

32 x 32 GPR

ALU

MAC

Timers

(FIT, PIT, Watchdog)

Timers & Debug

Debug Logic

JTAG

Instruction Trace
Integrated Software Environment (ISE)

Used for generating configuration bitstream.
http://www.xilinx.com/ise/logic_design_prod/webpack.htm
Webpack is subset of “Foundation” version.

Good tutorial for version 8.1:

Using Makefiles:
http://www.xess.com/appnotes/makefile.html
### ISE versions

<table>
<thead>
<tr>
<th>Webpack</th>
<th>Foundation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Free of charge, Support only for simple boards</td>
<td>Usually requires payment, but: LS12 has licenses that can be temporarily assigned to students if they sign an NDA.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Webpack 9.1i (Jan. 2007)</th>
<th>Foundation 9.1i (Dec. 2006)</th>
</tr>
</thead>
<tbody>
<tr>
<td>No longer available</td>
<td>Pre-installed for lab of this course Includes Modelsim full VHDL simulator (always fast) 2.5 GB (file size)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Webpack 10.1i</th>
<th>Foundation 10.1i</th>
</tr>
</thead>
<tbody>
<tr>
<td>No support for our boards</td>
<td>Currently only ISE available to us, only 60 days trial license for EDK</td>
</tr>
</tbody>
</table>

Downloadable via www.xilinx.com includes simple VHDL simulator + optional version of Modelsim full VHDL simulator (slow for large files)
Start window

No project is open
Select:
File>Open Project
or
File>New Project

No flow available.
New Project

New Project Wizard - Create New Project

Enter a Name and Location for the Project

Project Name: bla
Project Location: C:\marwedel\lehre\eda\06-ss\bla

Select the Type of Top-Level Source for the Project

Top-Level Source Type: HDL

More Info  < Back  Next >  Cancel
Properties

Our device family is called Virtex2P.
Creating a new VHDL module ...
Defining I/O ports
Generated VHDL template
Defining the behavior ...
Checking syntax ...

Double click on check syntax
Synthesizing the design ...

Double click on synthesize
Implementing the design ...

Double click on "implement design"
Defining I/O pin constraints ...

Generate new source and click on implementation constraints
Click on assign package pins
Click on package view
Enter constraints according to list on earlier slide

Drag and drop of box in leftmost column to appropriate cycle in the layout;
Adjust I/O standard
Summary

- **Our board:**
  XUP V2P board: XCV2P30 FPGA, lots of peripherals.

- **XCV2P30 properties**
  - 80x46 CLBs and
  - Local RAM
  - Multipliers
  - 2 PowerPC processors

- **ISE development software**
  ISE accepts behavioral descriptions in VHDL
  Synthesis and implementation tool steps.
  Pin constraint editor.
  ISE webpack available for everyone free of charge