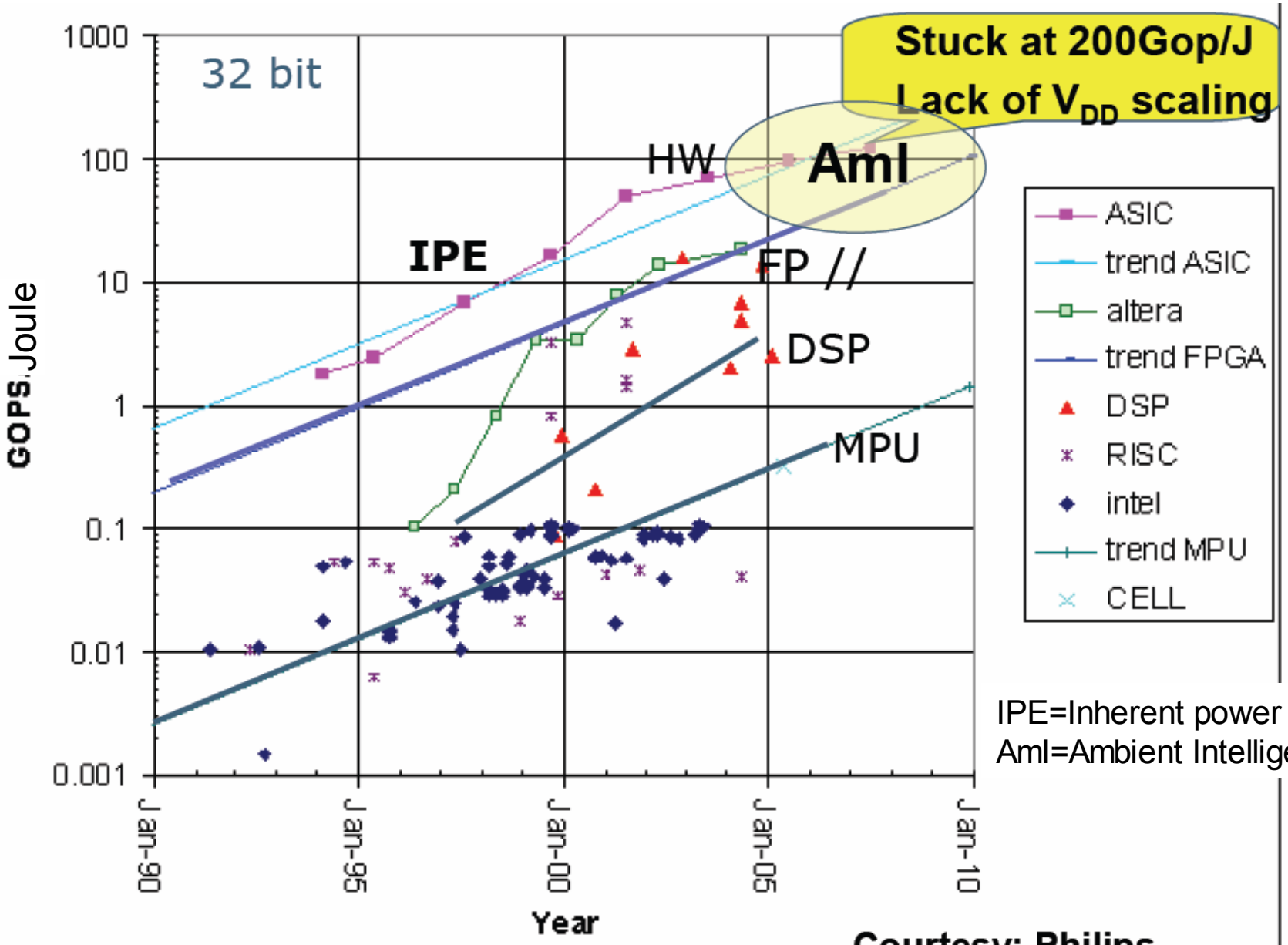
FPGA-Programming

P. Marwedel
Informatik 12, U. Dortmund

Importance of Energy Efficiency

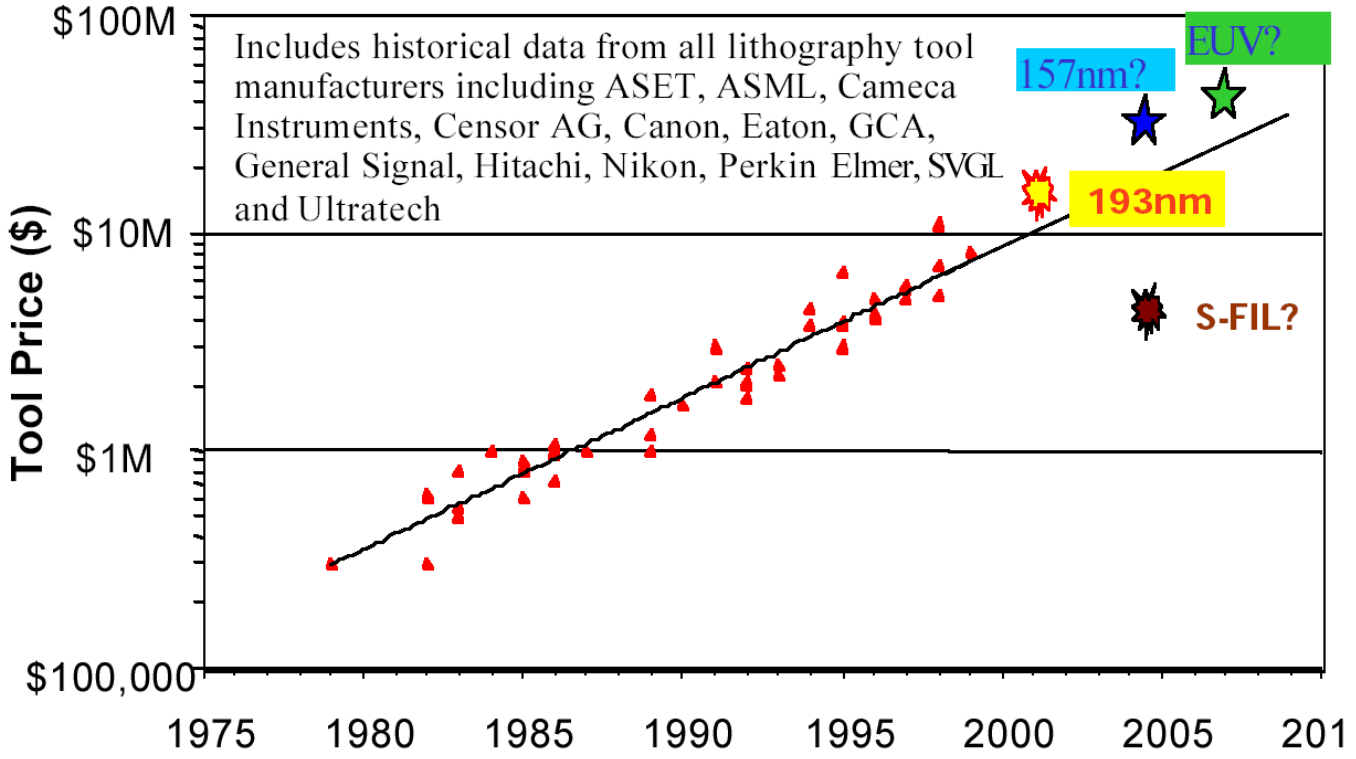


Courtesy: Philips
© Hugo De Man, IMEC, 2007

IPE=Inherent power efficiency
AmI=Ambient Intelligence

Challenges for implementation in hardware

- Lack of flexibility (changing standards).
- Mask cost for specialized HW becomes very expensive



Special hardware is ruled out for many applications, but energy efficiency is still required.

[http://www.molecularimprints.com/Technology/tech_articles/MII_COO_NIST_2001.PDF9]

Reconfigurable Logic

Full custom chips may be too expensive, software too slow.

- ☞ Combine the speed of HW with the flexibility of SW
- ☞ HW with programmable functions and interconnect.
- ☞ Use of configurable hardware;
  common form: field programmable gate arrays (FPGAs)

Applications: bit-oriented algorithms like

- encryption,
- fast „object recognition“ (medical and military),
- Adapting mobile phones to different standards.

Very popular devices from

- XILINX (e.g. XILINX Vertex II)
- Actel and others

Gliederung

Zeitplan

- Einführung
- SystemC
  - Vorlesungen und Programmierung

3,5 Wochen

- FPGAs
  - Vorlesungen
  - VHDL-basierte Konfiguration von FPGAs mit dem XUP VII Pro Entwicklungssystem

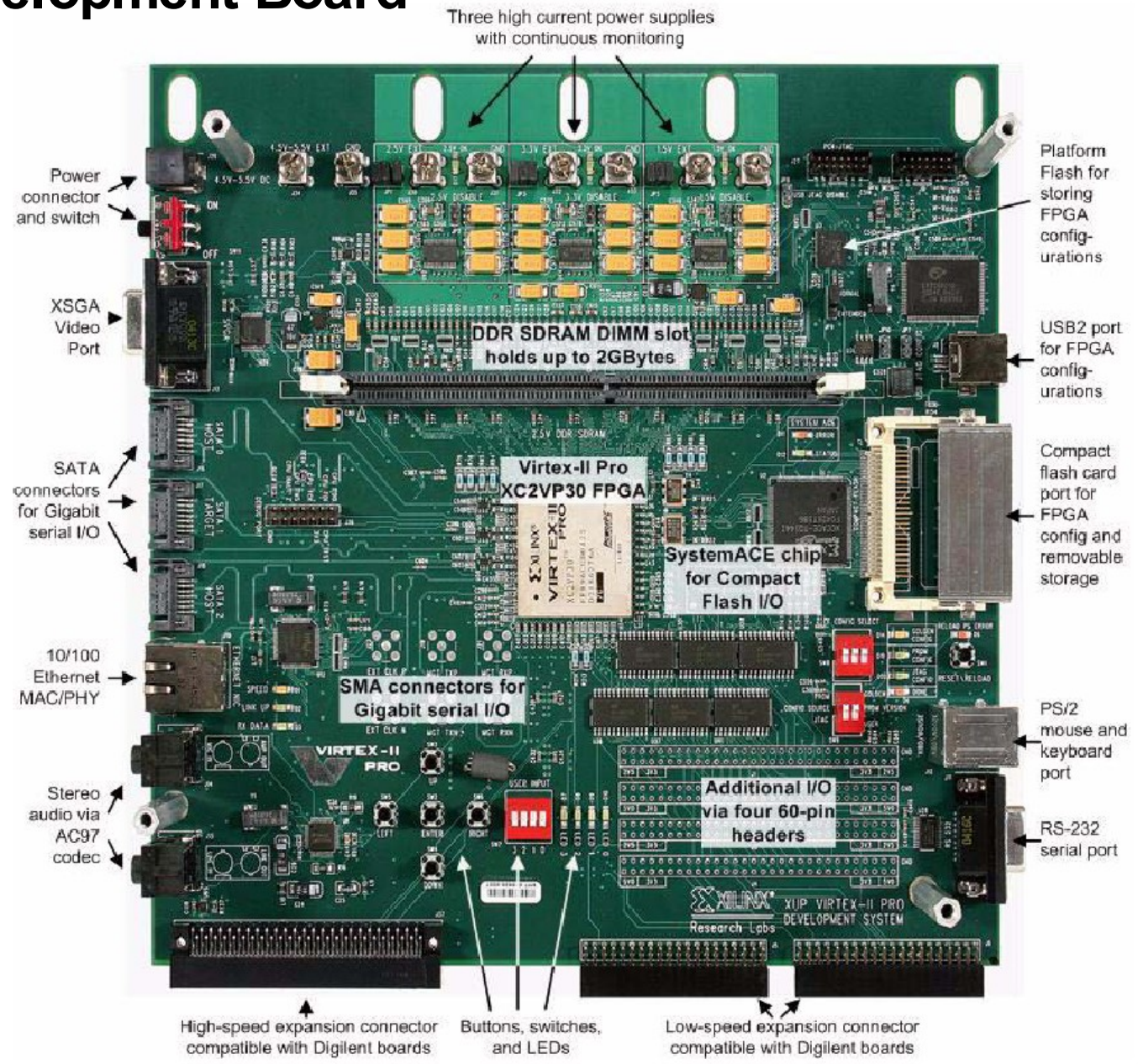
3,5 Wochen

- Algorithmen
  - Mikroarchitektur-Synthese
  - Automatensynthese
  - Logiksynthese
  - Layoutsynthese

6 Wochen

Xilinx University Program (XUP) Virtex II Pro Development Board

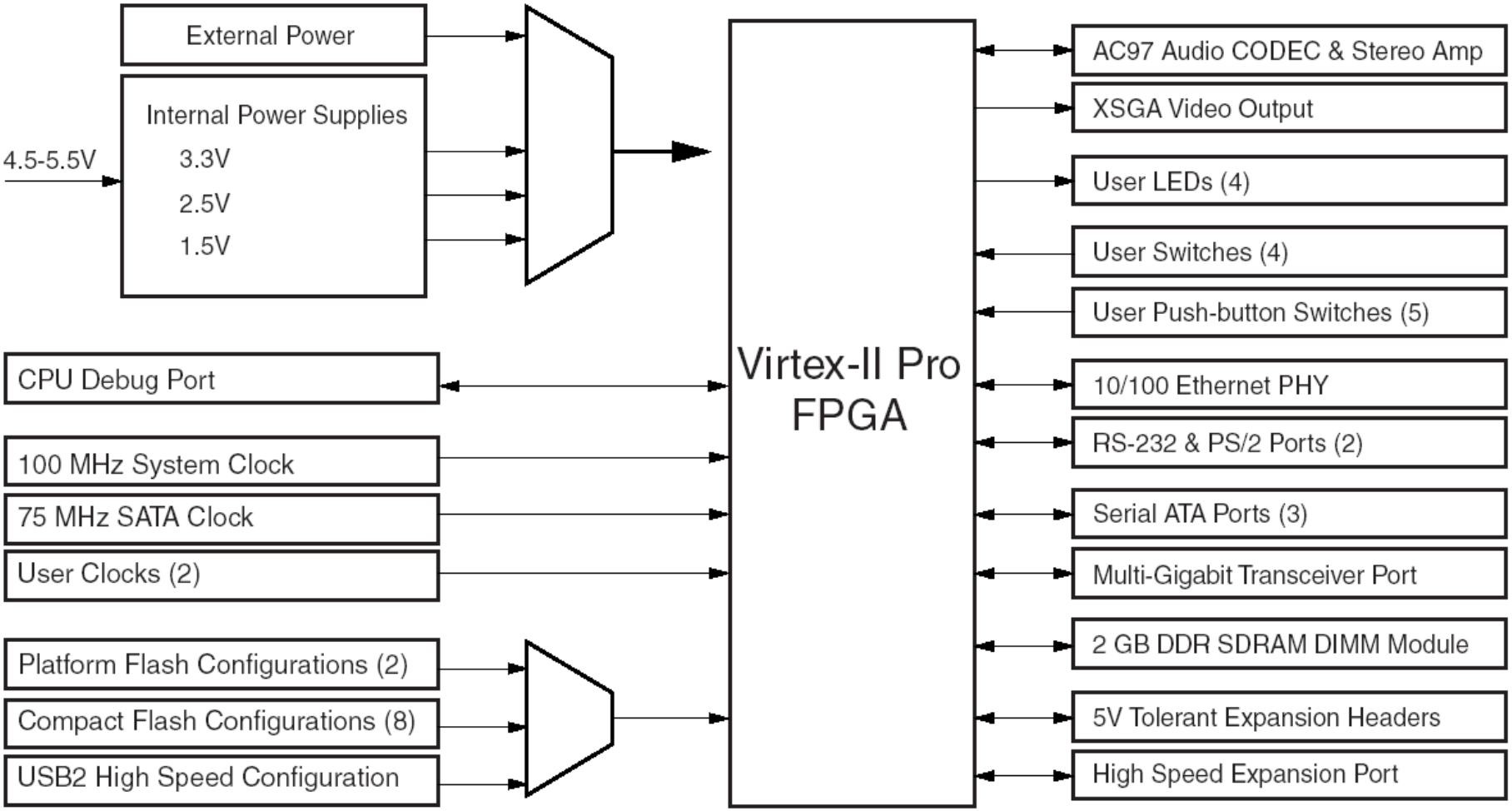
We are using a large board of the XUP line.



http://www.xilinx.com/xlnx/xweb/xil_publications_display.jsp?iLanguageID=1&category=-1212168&sGlobalNavPick=&sSecondaryNavPick=

Xilinx University Program (XUP)
Virtex II Pro Development Board

The board includes a good number of I/O interfaces.



Properties of the Virtex™-II Pro board (1)

- Virtex™-II Pro FPGA with PowerPC™ 405 cores
- Up to 2 GB of Double Data Rate (DDR) SDRAM
- System ACE™ controller and Type II CompactFlash™ connector for FPGA configuration and data storage
- Embedded Platform Cable USB configuration port
- High-speed SelectMAP FPGA configuration from Platform Flash In-System
- Programmable Configuration PROM
- Support for “Golden” and “User” FPGA configuration bitstreams
- On-board 10/100 Ethernet PHY device
- Silicon Serial Number for unique board identification
- RS-232 DB9 serial port
- Two PS-2 serial ports
- Four LEDs connected to Virtex-II Pro I/O pins
- Four switches connected to Virtex-II Pro I/O pins
- Five push buttons connected to Virtex-II Pro I/O pins

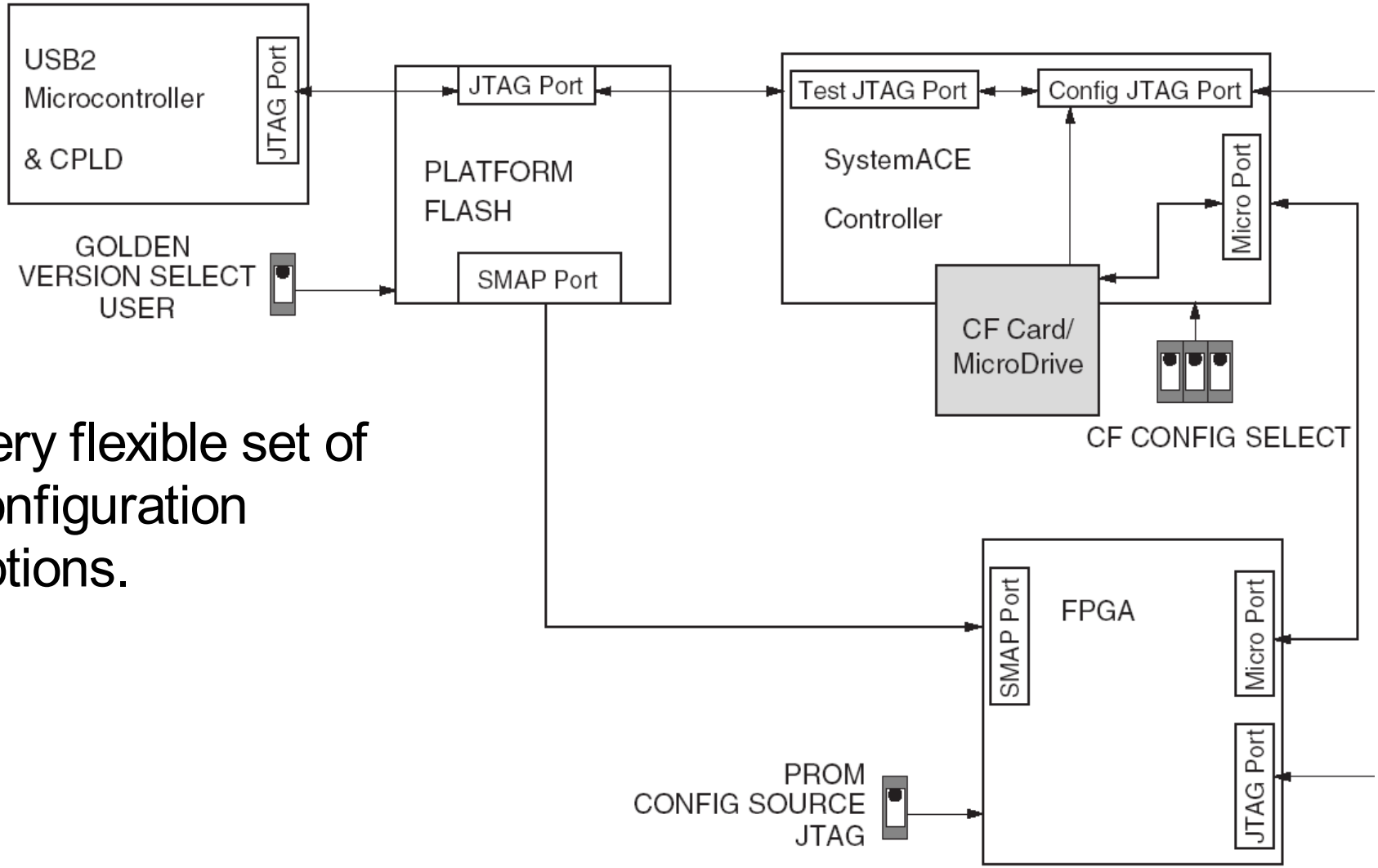
Properties of the Virtex™-II Pro board (2)

- Six expansion connectors joined to 80 Virtex-II Pro I/O pins with over-voltage protection
- High-speed expansion connector joined to 40 Virtex-II Pro I/O pins that can be used differentially or single ended
- AC-97 audio CODEC with audio amplifier and speaker/headphone output and line level output
- Microphone and line level audio input
- On-board XSGA output, up to 1200 x 1600 at 70 Hz refresh
- Three Serial ATA ports, two Host ports and one Target port
- Off-board expansion MGT link, with user-supplied clock
- 100 MHz system clock, 75 MHz SATA clock
- Provision for user-supplied clock
- On-board power supplies
- Power-on reset circuitry
- PowerPC 405 reset circuitry

User LED and switch connections

Signal	Direction	FPGA Pin	I/O Type	Drive	Slew
LED_0	O	AC4	LVTTL	12 mA	SLOW
LED_1	O	AC3	LVTTL	12 mA	SLOW
LED_2	O	AA6	LVTTL	12 mA	SLOW
LED_3	O	AA5	LVTTL	12 mA	SLOW
SW_0	I	AC11	LVCMOS25	–	–
SW_1	I	AD11	LVCMOS25	–	–
SW_2	I	AF8	LVCMOS25	–	–
SW_3	I	AF9	LVCMOS25	–	–
PB_ENTER	I	AG5	LVTTL	–	–
PB_UP	I	AH4	LVTTL	–	–
PB_DOWN	I	AG3	LVTTL	–	–
PB_LEFT	I	AH1	LVTTL	–	–
PB_RIGHT	I	AH2	LVTTL	–	–

Configuration data path



Very flexible set of configuration options.

Selecting the proper initialization (1)

(Power up) or (RESET_RELOAD (SW1) pressed for >2 s: FPGA begins configuring
2 configuration methods, selected by CONFIG SOURCE switch (MSB (left) of SW9):

- If CONFIG SOURCE switch is *closed*, or *up:* high-speed SelectMap byte-wide configuration from on-board Platform Flash configuration PROM (U3) is selected, PROM CONFIG LED (D19) on.
  PROM supports 2 configs., selected by PROM VERSION switch = LSB of SW9.
  - PROM VERSION switch is *closed*, or *up:*
    GOLDEN config. from onboard Platform Flash configuration PROM selected, GOLDEN CONFIG LED (D14) = on.
    Config. can be board test utility provided by Xilinx.
    PROM VERSION switch sampled only at powerup and system reset.
    If switch changed later: RESET_RELOAD must be pressed for > 2 seconds.
  - PROM VERSION switch is *open*, or *down:* User configuration from the on-board Platform Flash configuration PROM is selected. This configuration **must** be programmed into the Platform Flash PROM from the JTAG Platform Cable USB interface or the USB interface following the instructions in Appendix B.

  Platform Flash is normally disabled after configuring (DONE='1').
  If additional data to be read, jumper JP9 must be moved to EXTENDED.
  FPGA Start-Up Clock should be set to CCLK in the Startup Options section of the Process Options for the generation of the programming file.

Selecting the proper initialization (2)

- If CONFIG SOURCE switch is *open*, *off*, or *down,* a lower speed JTAG-based configuration from Compact Flash or external JTAG source is selected, JTAG CONFIG LED (D20)=on.
  - Default source is from the Compact Flash port (J7). If configuration data exists on the CF card, it becomes the source for the configuration data. The CF card supports up to eight different configuration data files, selected by the triple CF CONFIG SELECT DIP switch (SW8). During configuration, SYSTEMACE STATUS LED (D12) flashes. At completion: FPGA asserts the FPGA_DONE signal, DONE LED (D4) on. Any time: RESET_RELOAD on for >2 s: one of 8 configuration files loaded. D11 flashes if no *valid* configuration file is found on the Compact Flash card.
  - The high-speed embedded Platform Cable USB configuration port (J8) is enabled if no configuration is found on the CF card.

JTAG Clock should be selected in the Startup Options section of the Process Options for the generation of the programming file.

Number of resources available in Virtex II Pro devices

Table 16: **Virtex-II Pro Logic Resources Available in All CLBs**

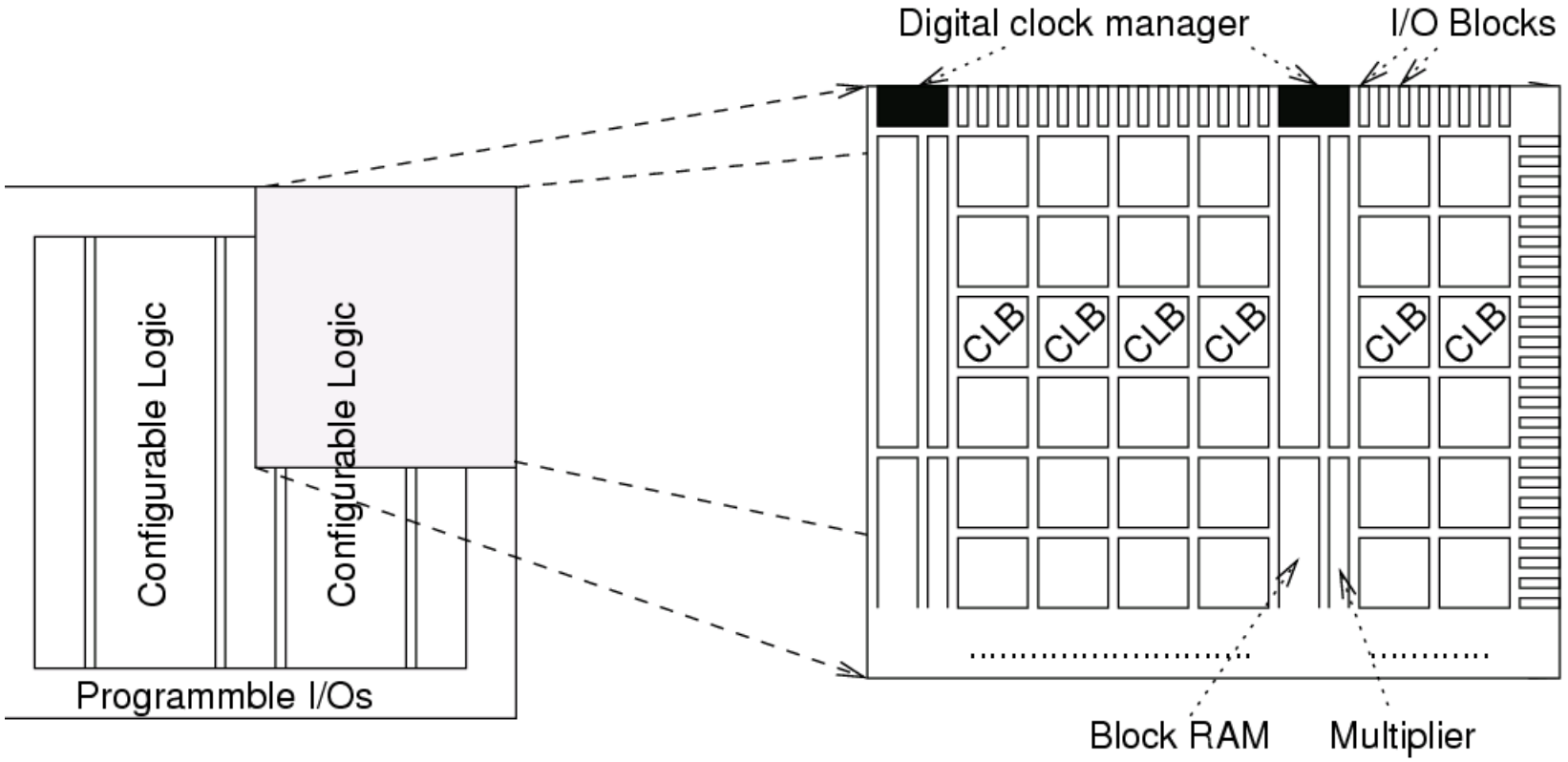
Device	CLB Array: Row x Column	Number of Slices	Number of LUTs	Max Distributed SelectRAM+ or Shift Register (bits)	Number of Flip-Flops	Number of Carry Chains(1)	Number of SOP Chains(1)
XC2VP2	16 x 22	1,408	2,816	45,056	2,816	44	32
XC2VP4	40 x 22	3,008	6,016	96,256	6,016	44	80
XC2VP7	40 x 34	4,928	9,856	157,696	9,856	68	80
XC2VP20	56 x 46	9,280	18,560	296,960	18,560	92	112
XC2VP30	80 x 46	13,696	27,392	438,272	27,392	92	160
XC2VP40	88 x 58	19,392	38,784	620,544	38,784	116	176
XC2VP50	88 x 70	23,616	47,232	755,712	47,232	140	176
XC2VP70	104 x 82	33,088	66,176	1,058,816	66,176	164	208
XC2VP100	120 x 94	44,096	88,192	1,411,072	88,192	188	240
XC2VP125	136 x 106	55,616	111,232	1,779,712	111,232	212	272

Notes:

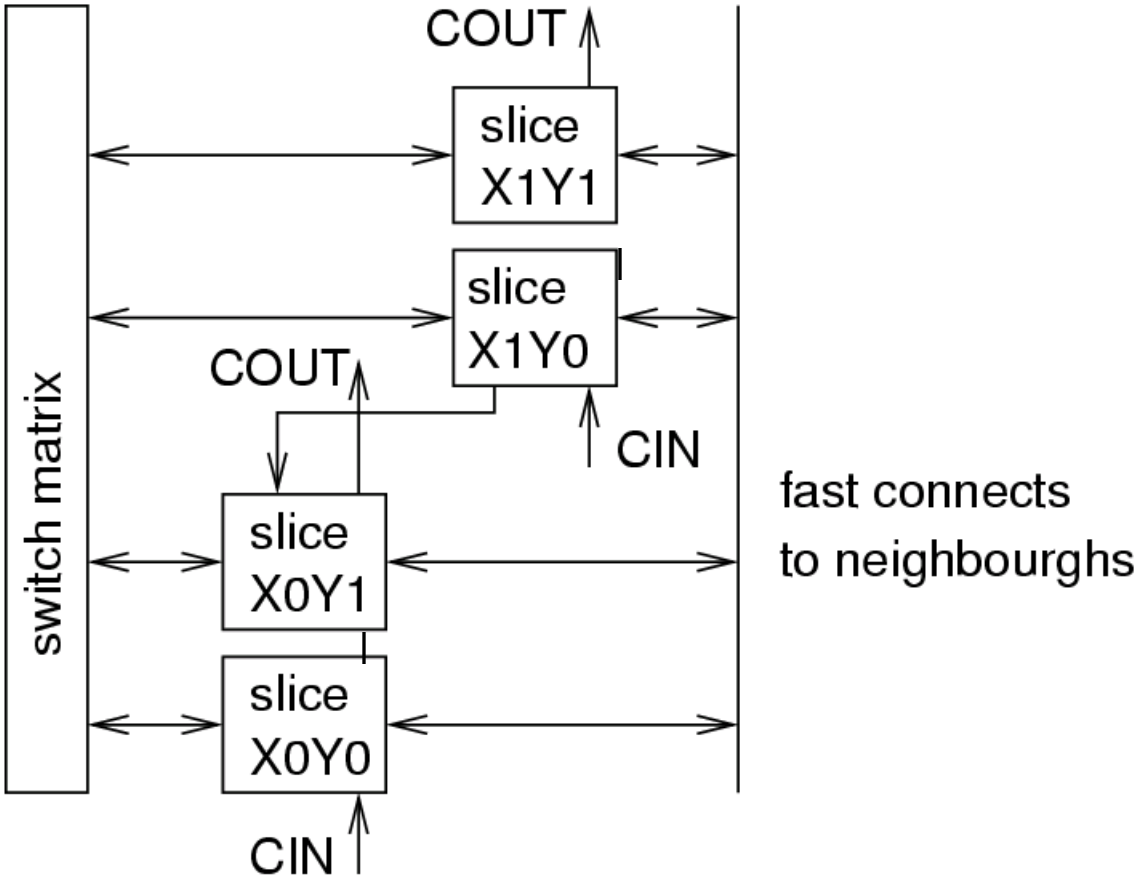
1. The carry-chains and SOP chains can be split or cascaded.

[© and source: Xilinx Inc.: Virtex-II Pro™ Platform FPGAs: Functional Description, Sept. 2002, //www.xilinx.com]

Floor-plan of VIRTEX II FPGAs

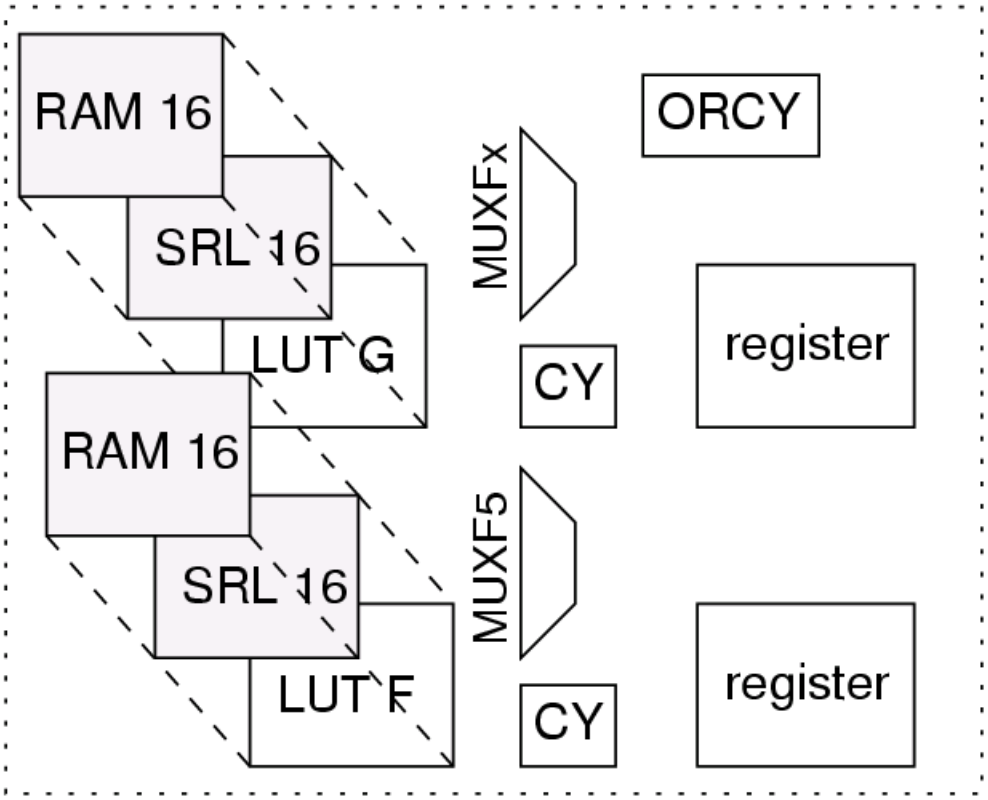


Virtex II Configurable Logic Block (CLB)



Virtex II Slice (simplified)

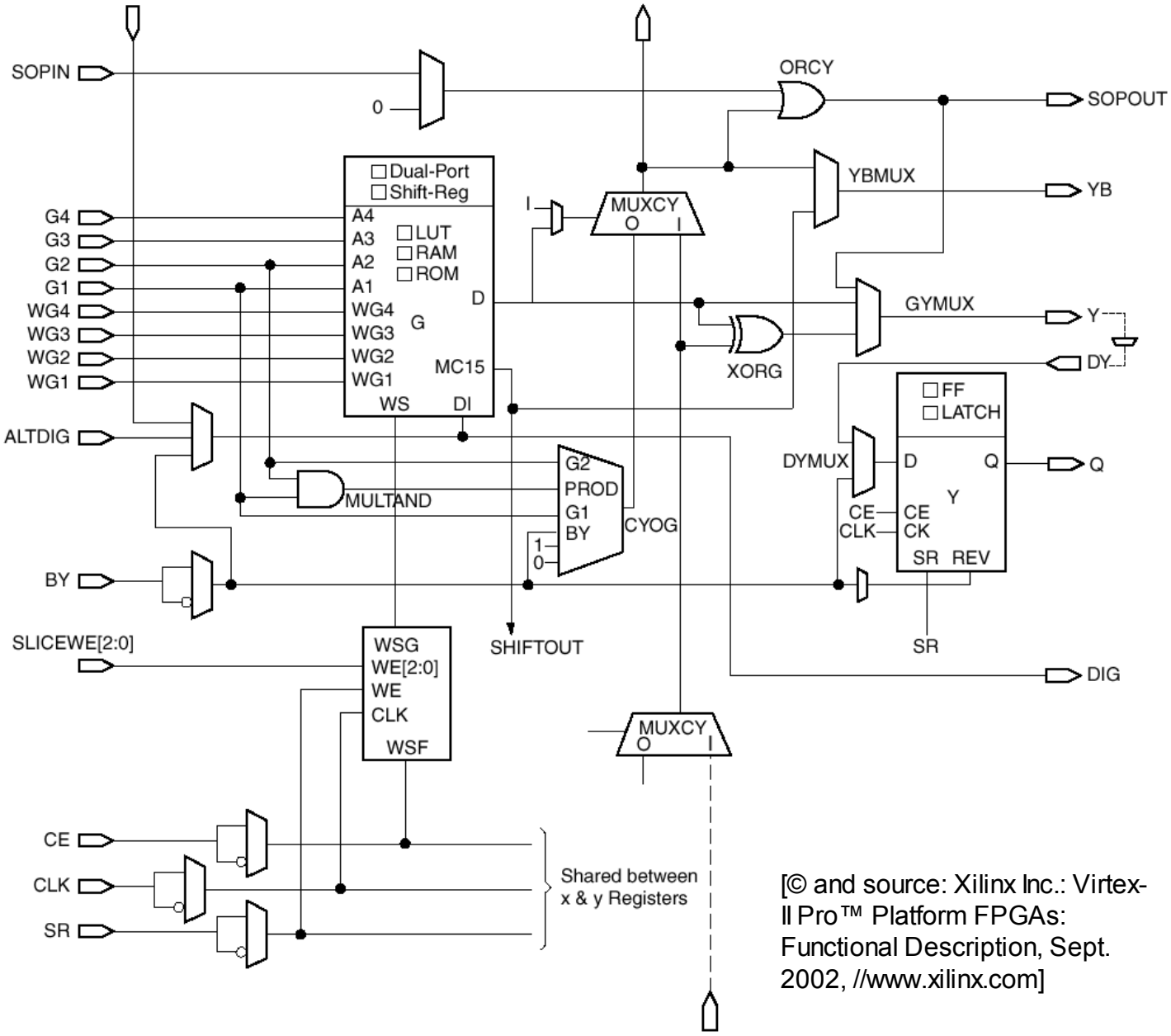
Look-up tables LUT F and G can be used to compute any Boolean function of ≤ 4 variables.



Example:

a	b	c	d	G
0	0	0	0	**0**
0	0	0	1	**1**
0	0	1	0	**1**
0	0	1	1	**0**
0	1	0	0	**1**
0	1	0	1	**0**
0	1	1	0	**0**
0	1	1	1	**1**
1	0	0	0	**1**
1	0	0	1	**0**
1	0	1	0	**0**
1	0	1	1	**1**
1	1	0	0	**0**
1	1	0	1	**1**
1	1	1	0	**1**
1	1	1	1	**0**

(½ of) Virtex II (Pro) Slice



[© and source: Xilinx Inc.: Virtex-II Pro™ Platform FPGAs: Functional Description, Sept. 2002, //www.xilinx.com]

2 carry paths per CLB (Vertex II Pro)

Enables efficient implementation of adders.

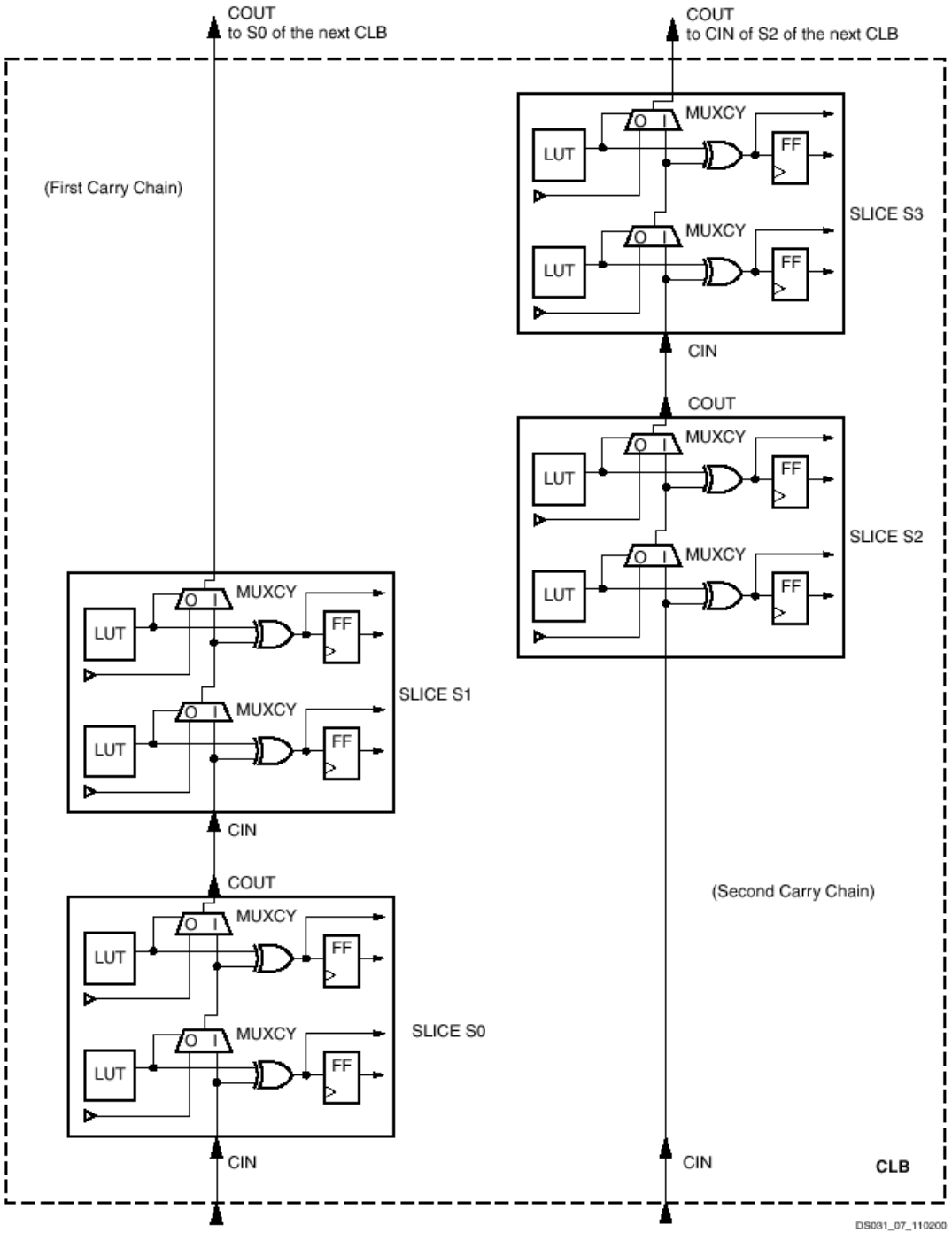


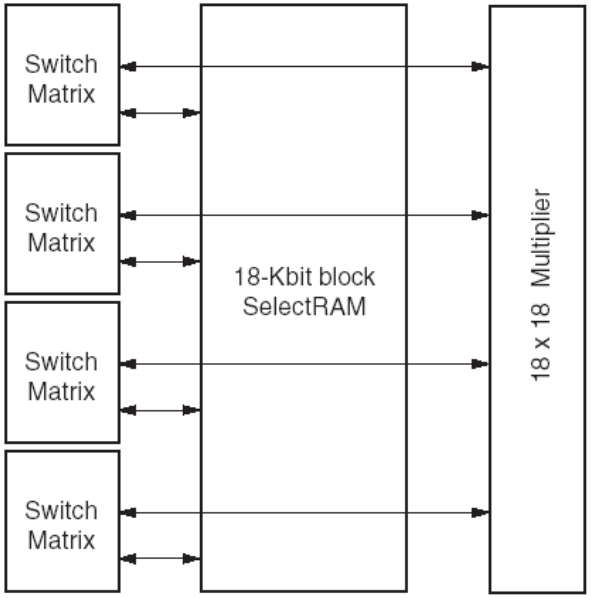
Figure 32: **Fast Carry Logic Path**

[© and source: Xilinx Inc.: Virtex-II Pro™ Platform FPGAs: Functional Description, Sept. 2002, //www.xilinx.com]

Embedded Multipliers

A Virtex-II Pro multiplier block is an 18-bit by 18- signed multiplier.

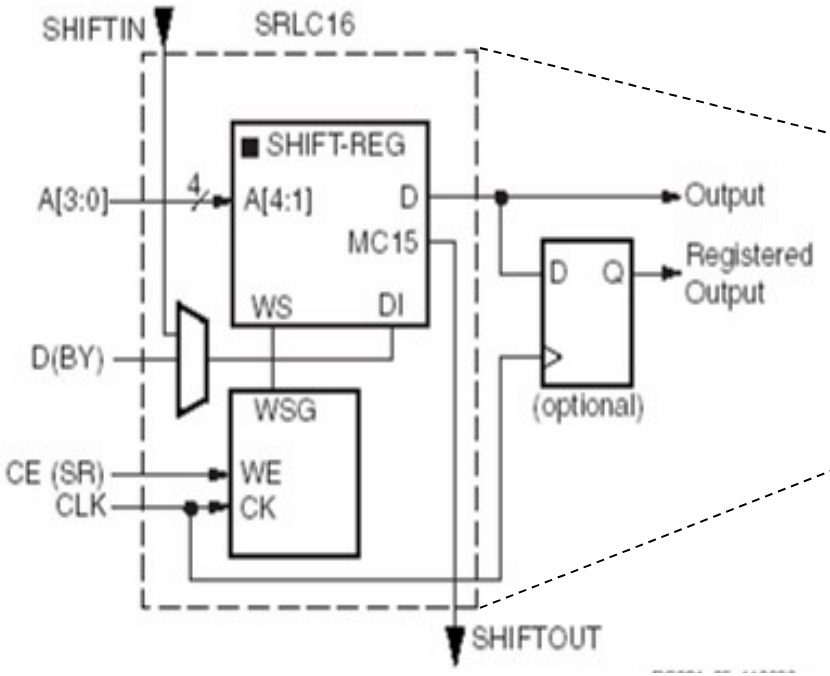
Multipliers are connected to a switch matrix, share some bits with RAM (☞MAC instruction).

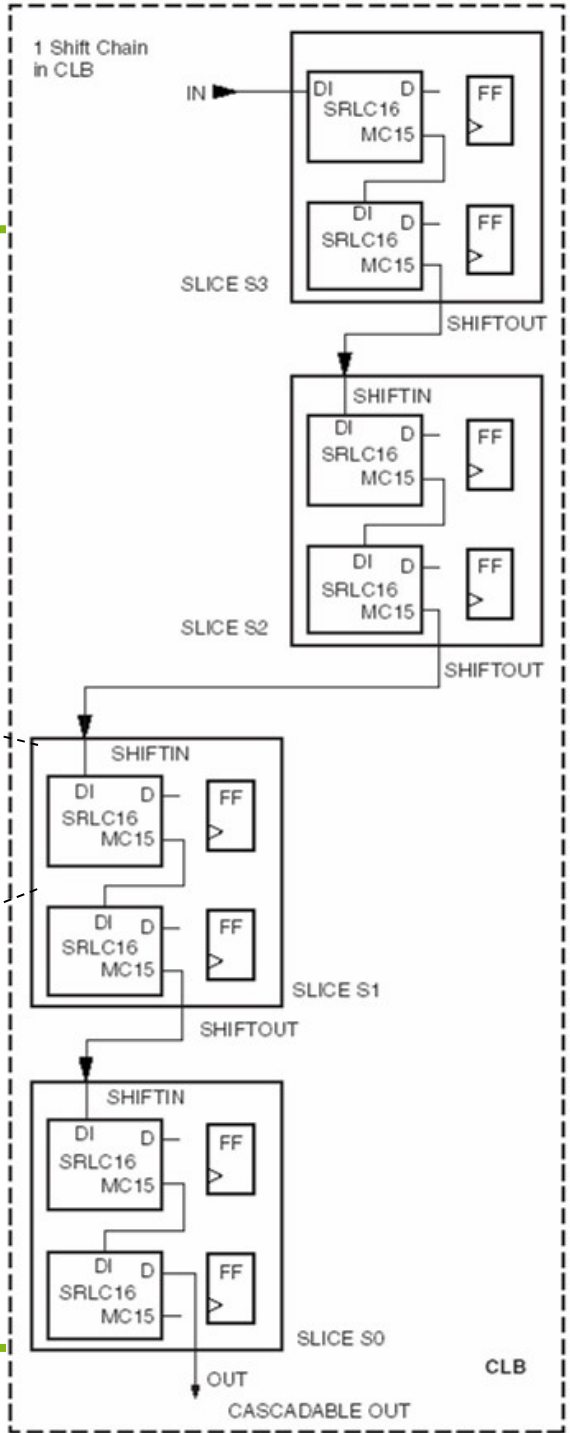


Device	Columns	Multipliers
XC2VP2	4	12
XC2VP4	4	28
XC2VP7	6	44
XC2VP20	8	88
XC2VP30	8	136
XC2VPX20	8	88
XC2VP40	10	192
XC2VP50	12	232
XC2VP70	14	328
XC2VPX70	14	308
XC2VP100	16	444

Shift register configuration

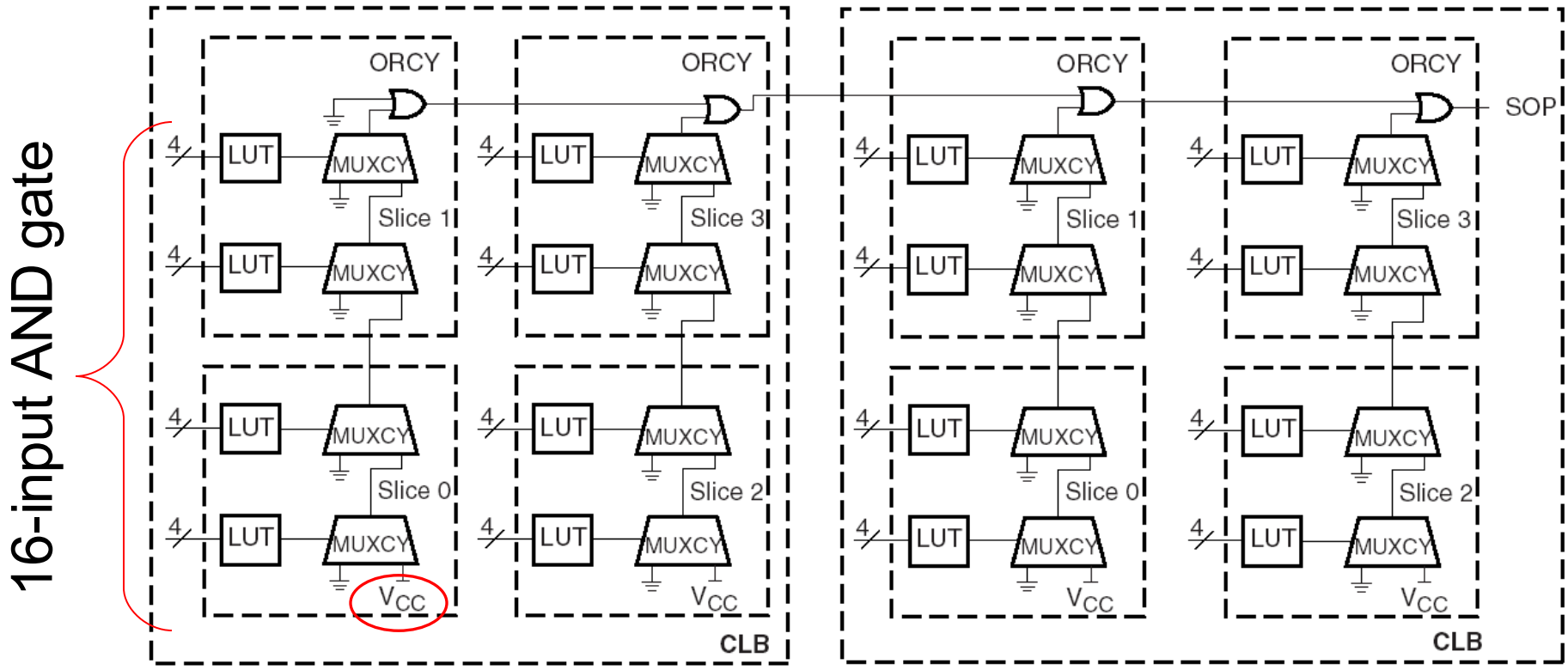
Slices can be configured as shift registers





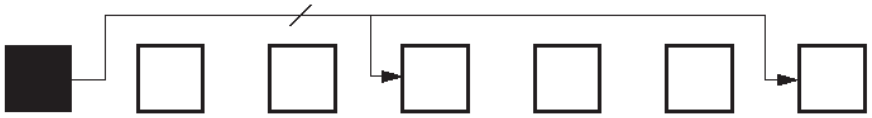
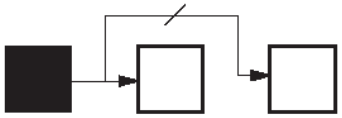
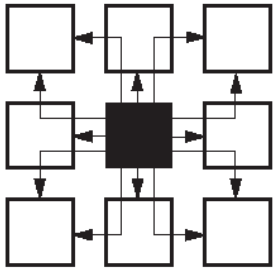
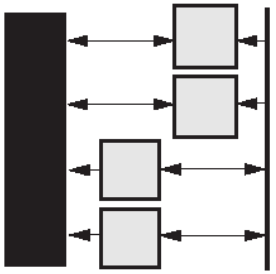
Implementing sums of products

Dedicated or chain for computing sum of products



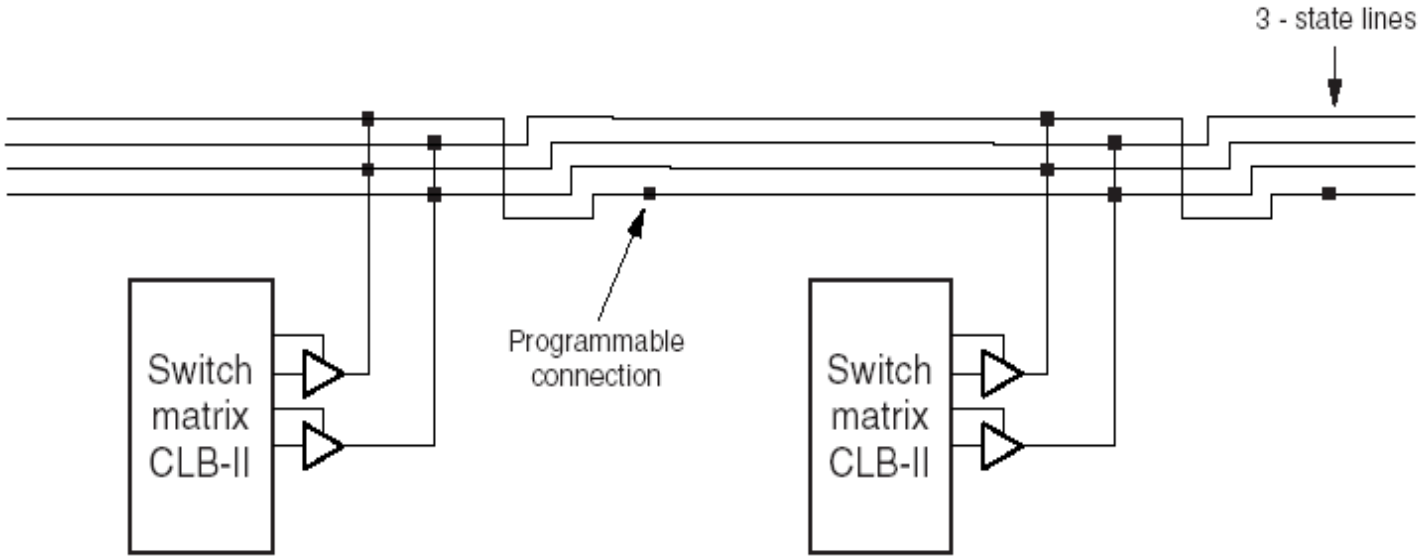
Interconnect

Hierarchical Routing Resources

24 Horizontal Long Lines 24 Vertical Long Lines	
120 Horizontal Hex Lines 120 Vertical Hex Lines	
40 Horizontal Double Lines 40 Vertical Double Lines	
16 Direct Connections (total in all four directions)	
8 Fast Connects	

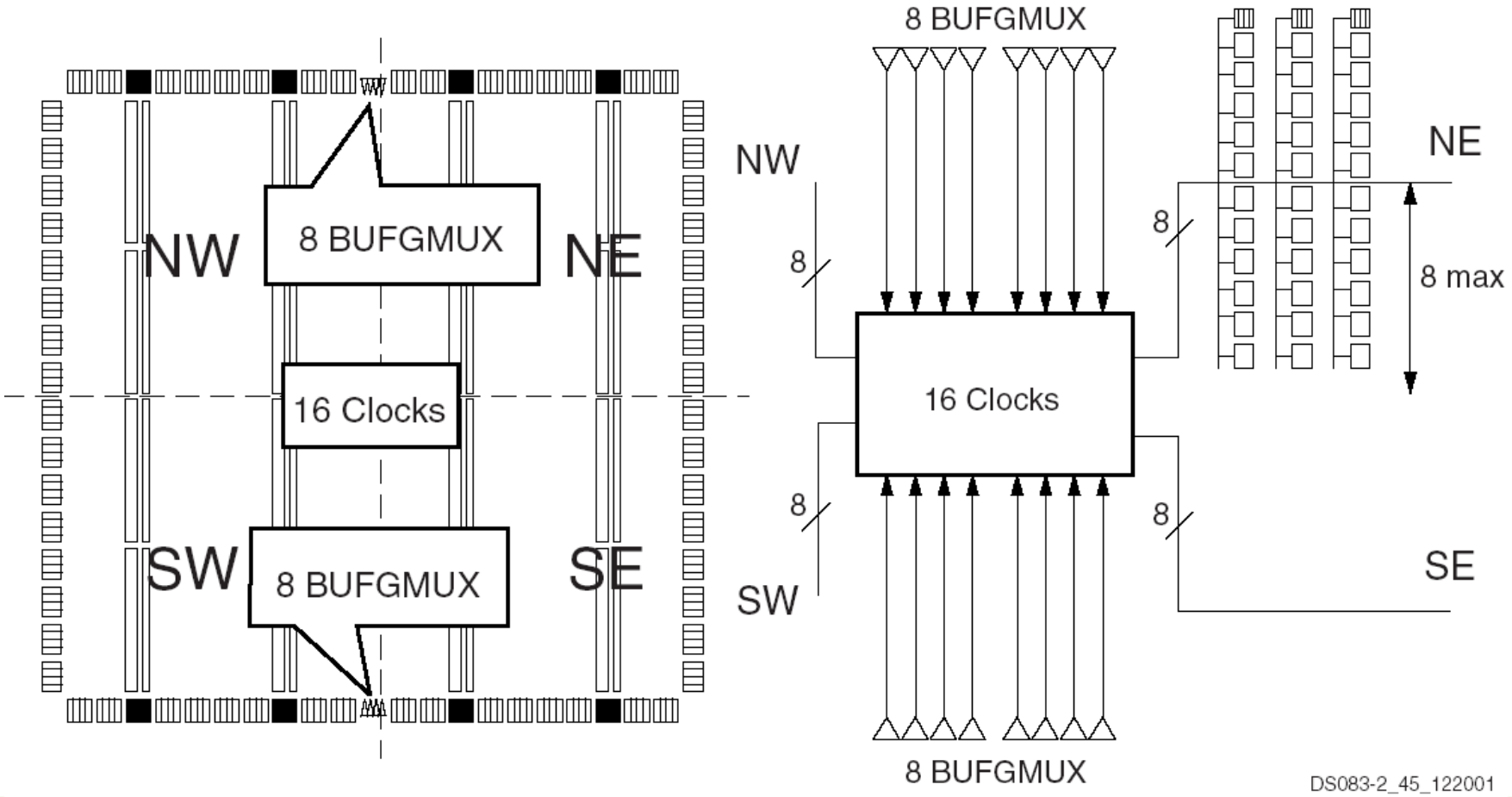
3-state buffers

Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row.

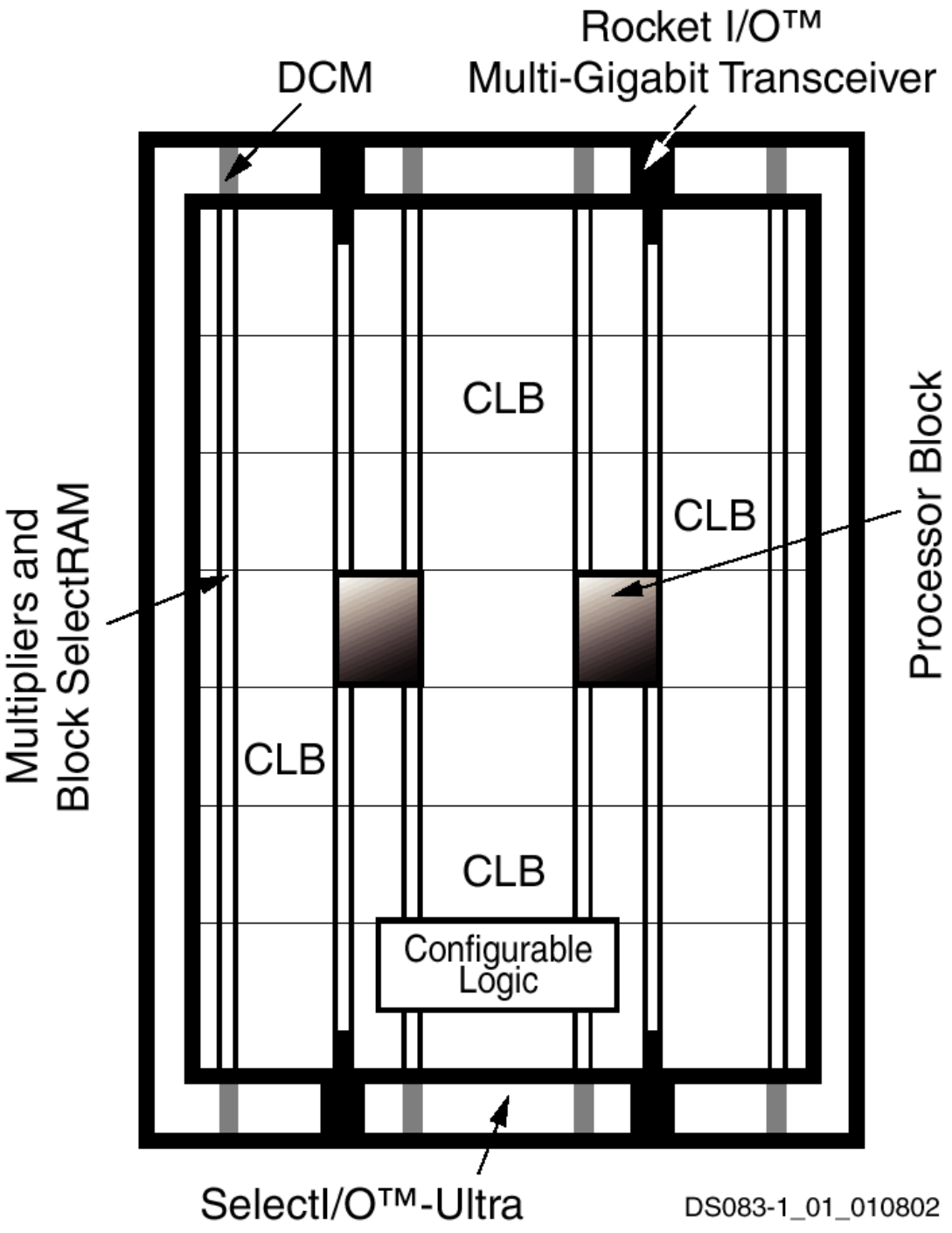


Clock distribution

Up to 16 global clocks are available.
≤ 8 clocks/quadrant can be used, organized in clock rows.



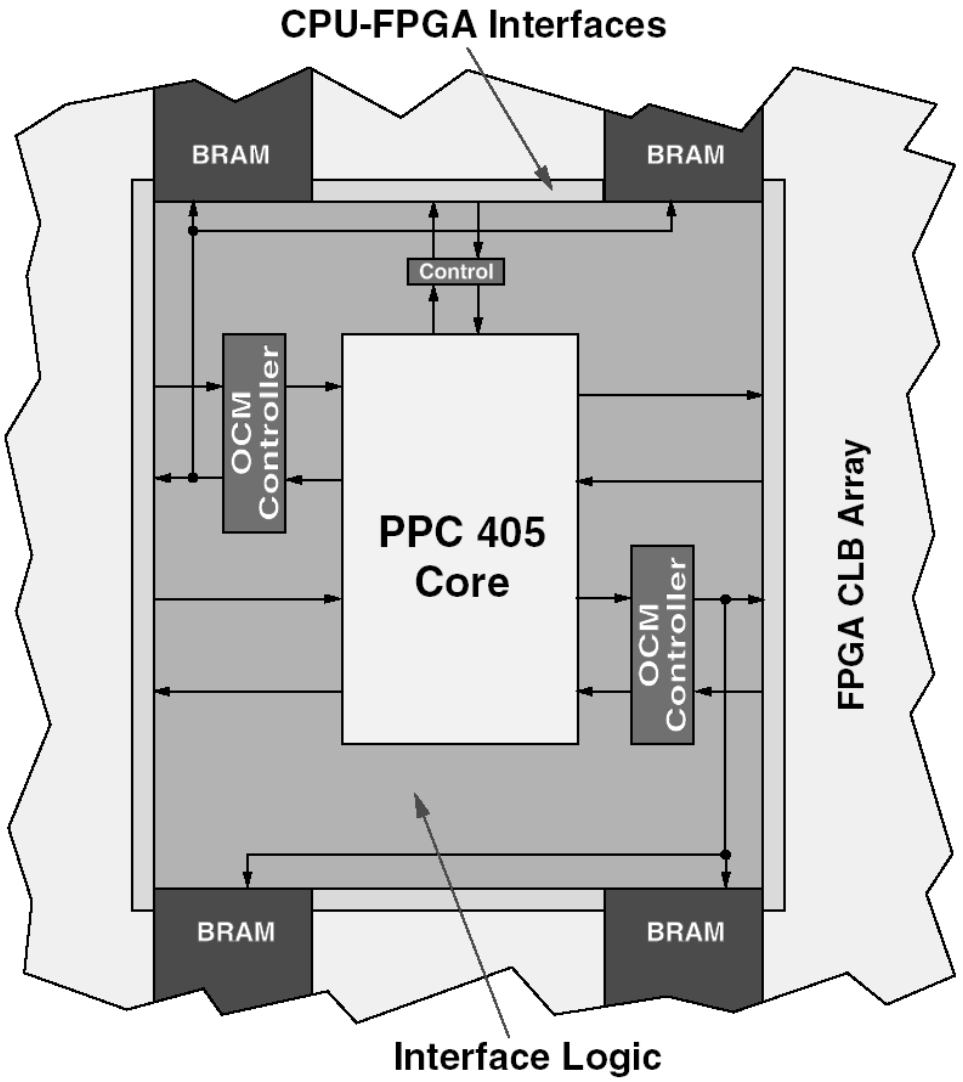
Virtex II Pro Devices include up to 4 PowerPC processor cores



[© and source: Xilinx Inc.: Virtex-II Pro™ Platform FPGAs: Functional Description, Sept. 2002, //www.xilinx.com]

Memory for processor cores

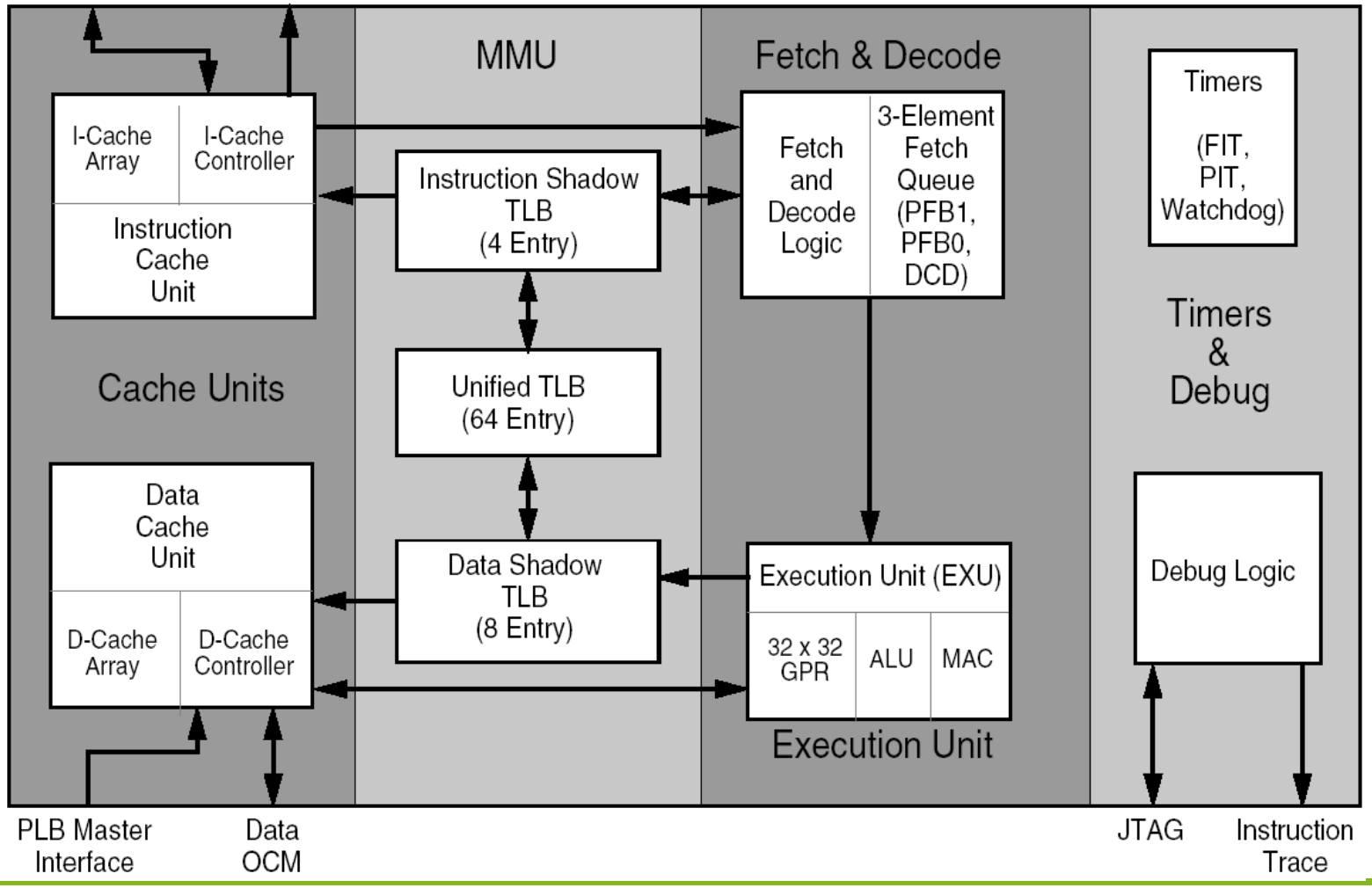
Cores are connected to local block RAM that can be used as a scratchpad.



Integrated PowerPC Processor

PLB=Processor local bus

OCM=on chip memory controller; interface to Block SelectRAM+ serving as scratch pad memory



Integrated Software Environment (ISE)

Used for generating configuration bitstream.

http://www.xilinx.com/ise/logic_design_prod/webpack.htm
Webpack is subset of “Foundation” version.

Good tutorial for version 8.1:
http://www.xess.com/appnotes/webpack-8_1-xsa.pdf

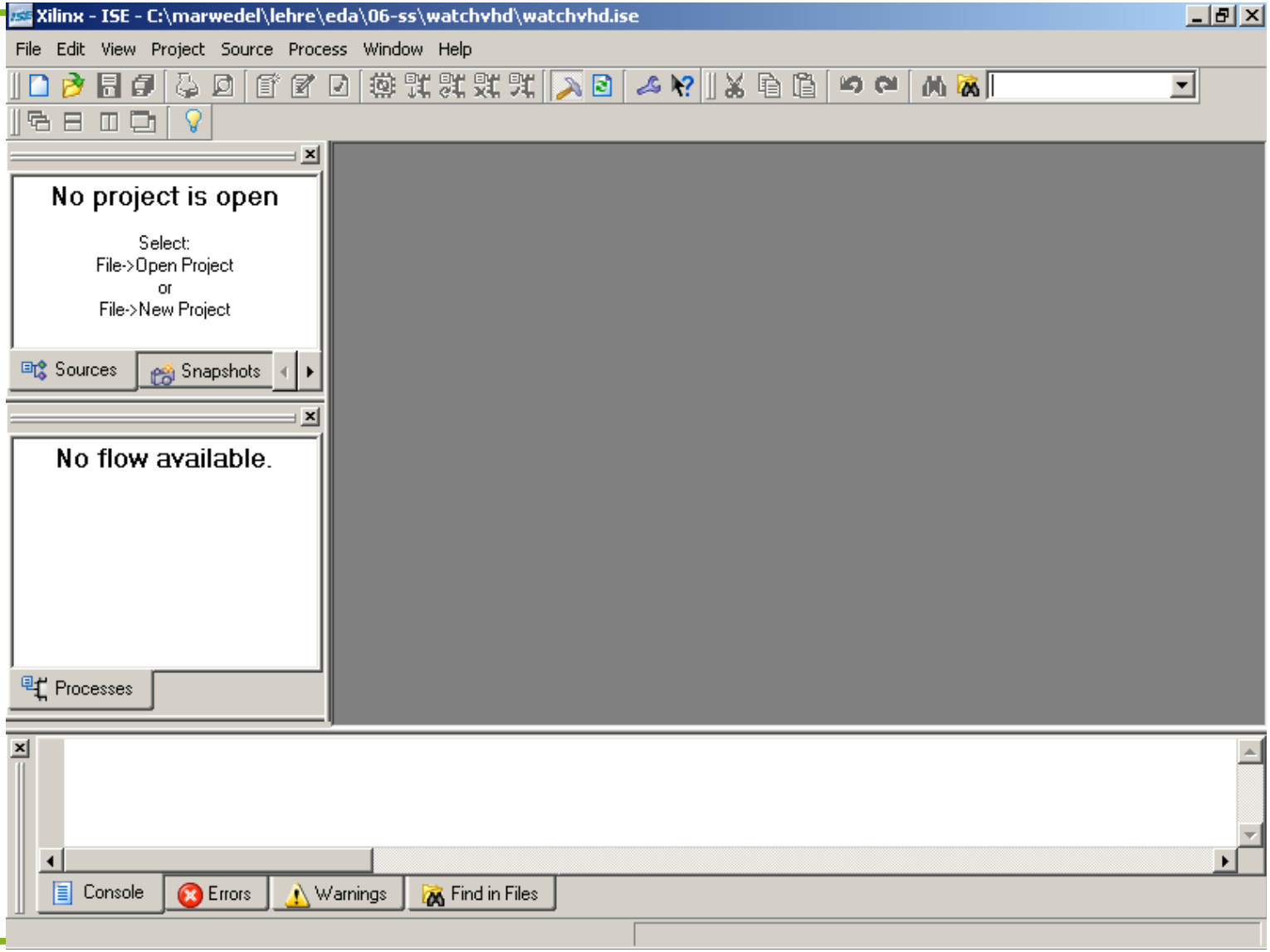
Using Makefiles:

http://www.xess.com/appnotes/makefile.html

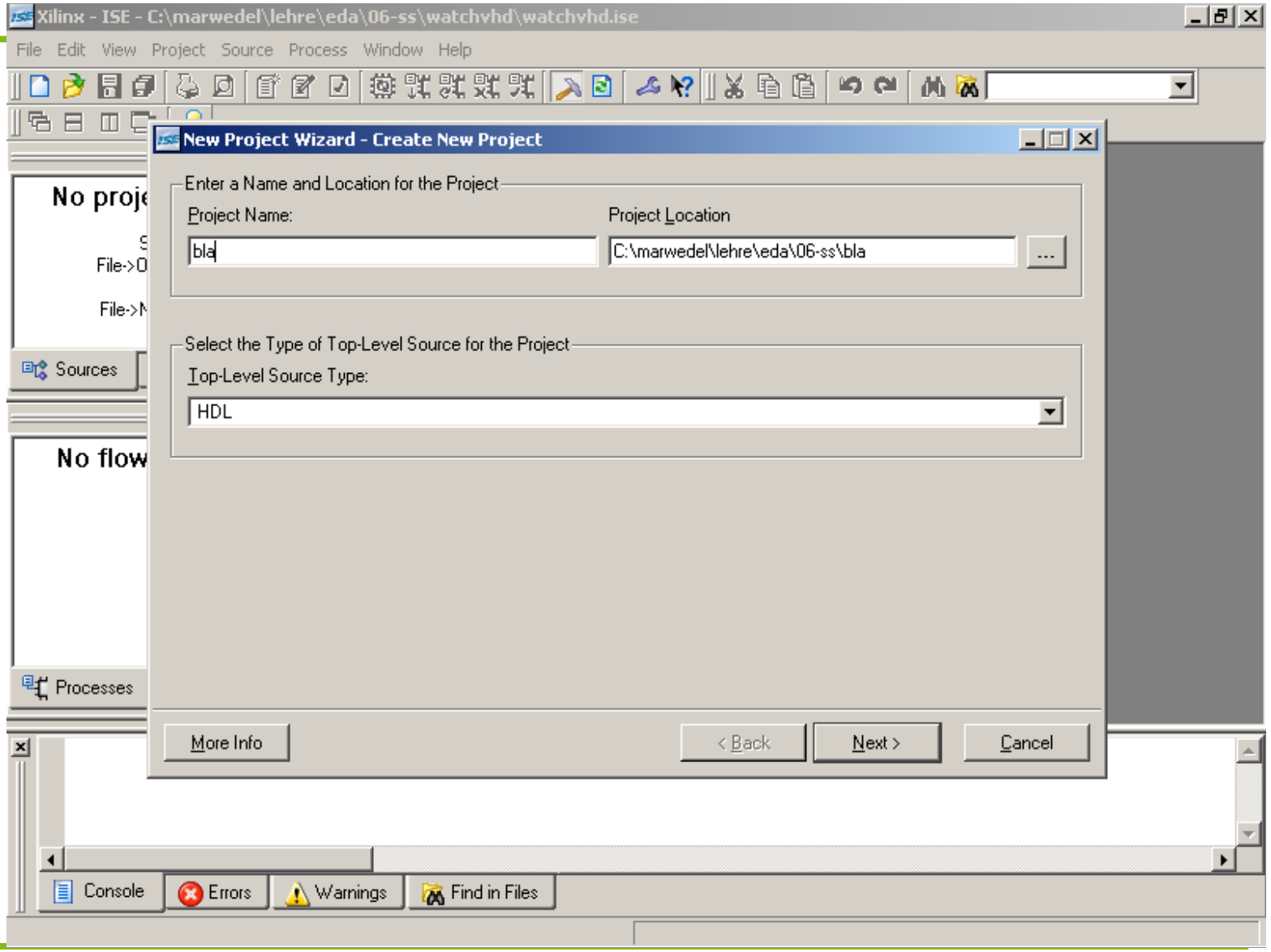
ISE versions

Webpack **Free of charge, Support only for simple boards**	***Foundation*** **Usually requires payment, but:** LS12 has licenses that can be temporarily assigned to students if they sign an NDA.
Webpack 9.1i (Jan. 2007)	*Foundation 9.1i* (Dec. 2006)
No longer available	Pre-installed for lab of this course Includes Modelsim full VHDL simulator (always fast) 2.5 GB (file size)
Webpack 10.1i	*Foundation 10.1i*
No support for our boards	
Downloadable via www.xilinx.com includes simple VHDL simulator + optional version of Modelsim full VHDL simulator (slow for large files)	Currently only ISE available to us, only 60 days trial license for EDK

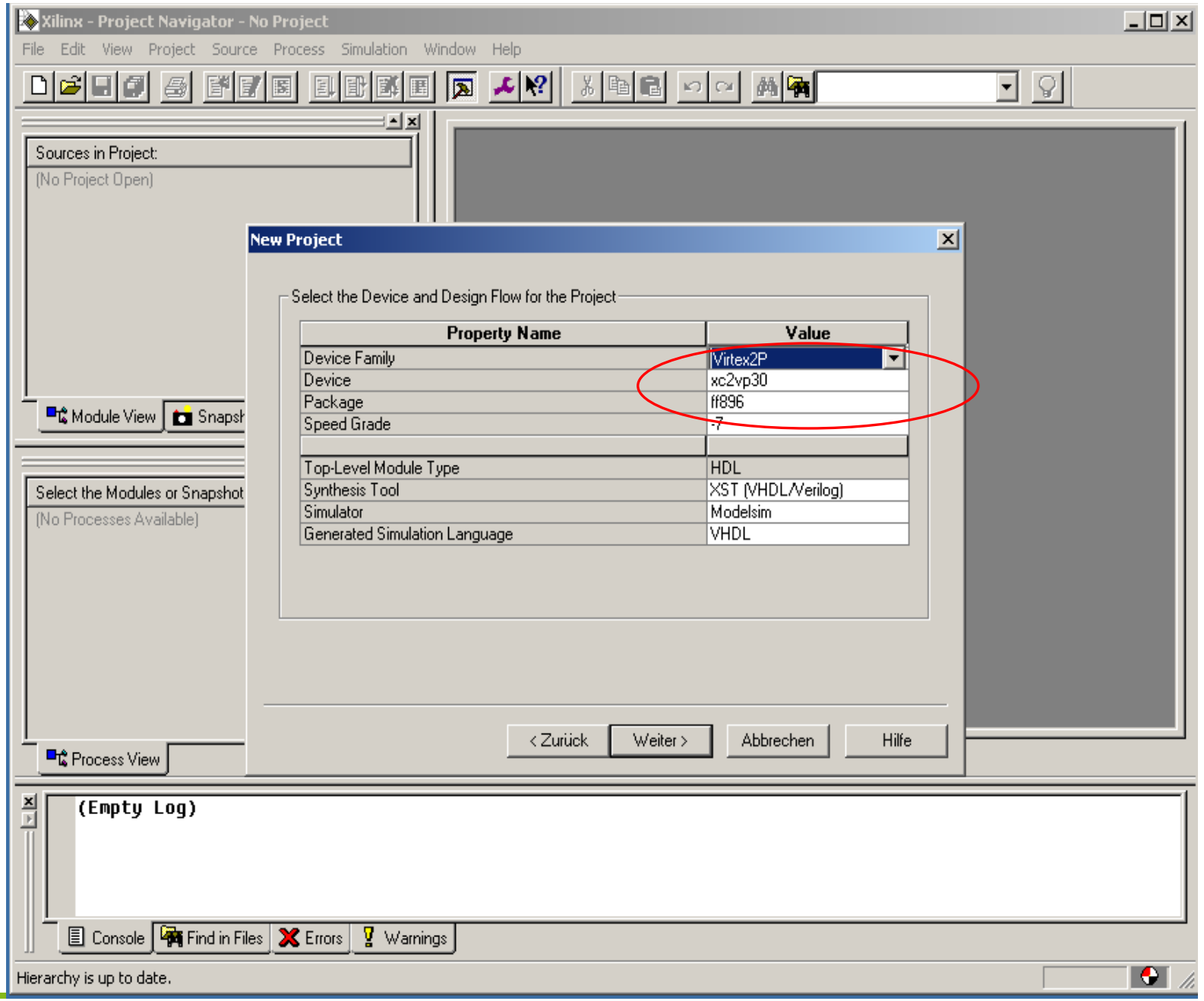
Start window



New Project

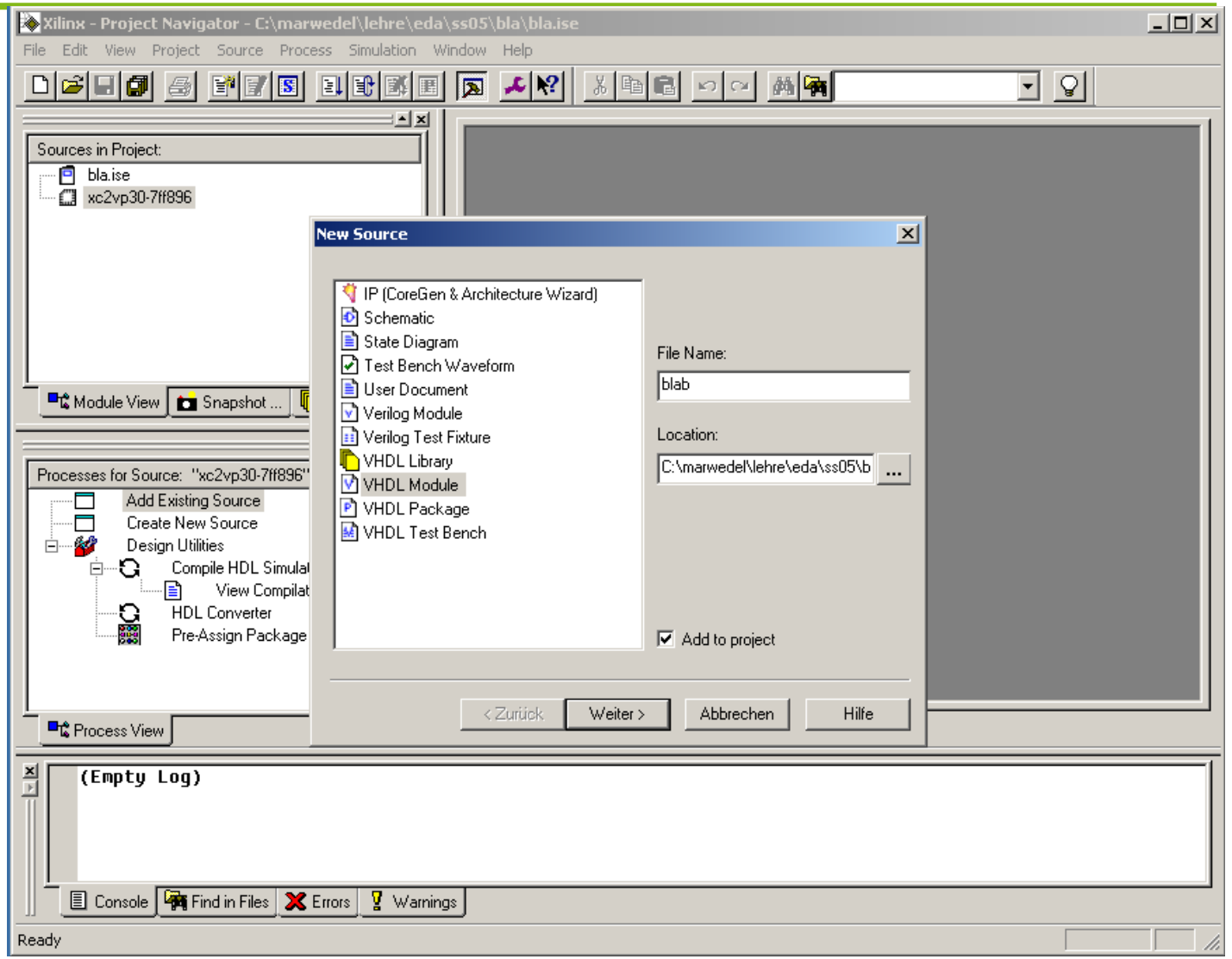

Xilinx - ISE - C:\marwedel\lehre\eda\06-ss\watchvhd\watchvhd.ise
File Edit View Project Source Process Window Help
New Project Wizard - Create New Project
Enter a Name and Location for the Project
Project Name:
bla
Project Location
C:\marwedel\lehre\eda\06-ss\bla
...
Select the Type of Top-Level Source for the Project
Top-Level Source Type:
HDL
More Info
< Back
Next >
Cancel
Sources
Processes
Console
Errors
Warnings
Find in Files

Properties

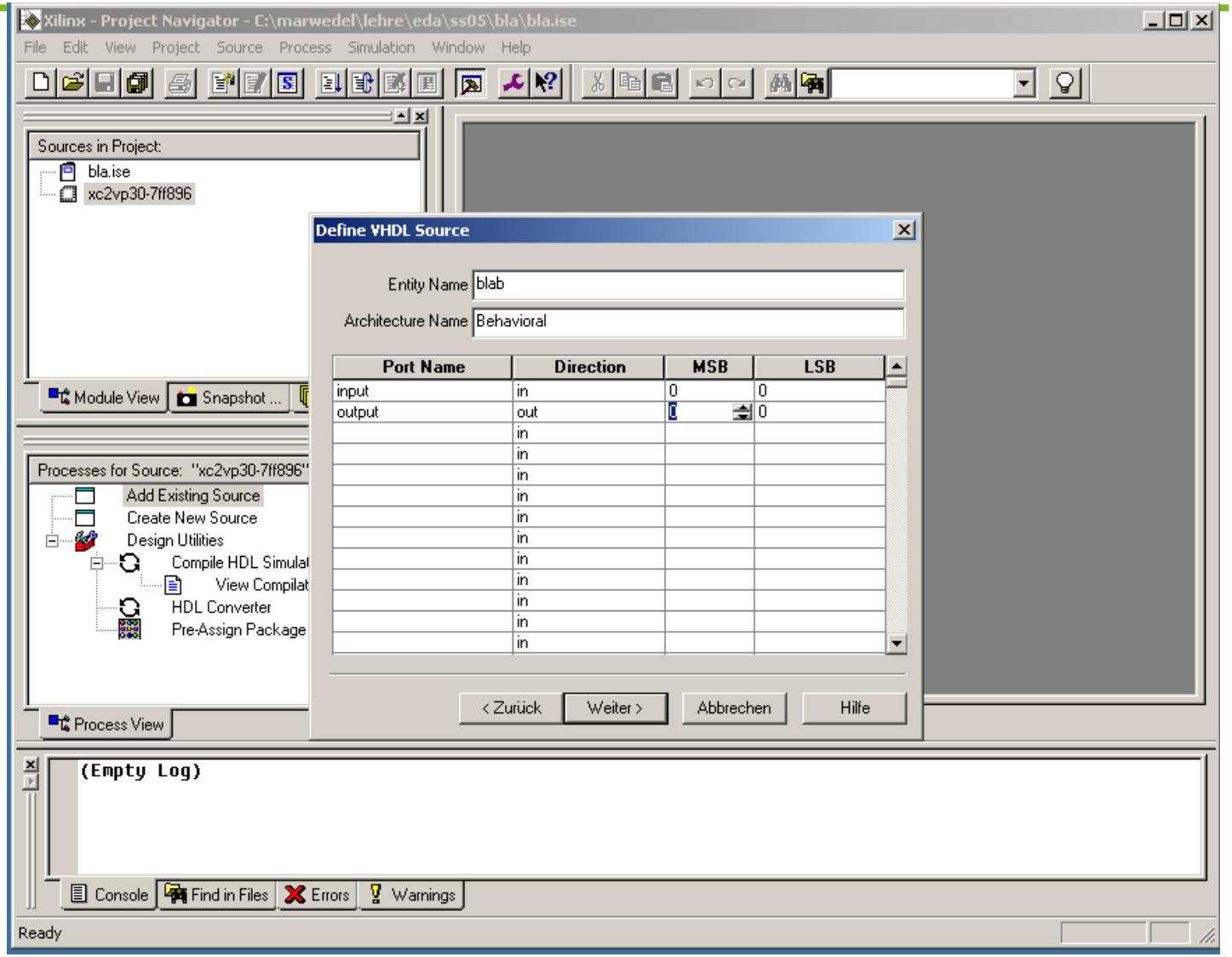


Our device family is called Virtex2P

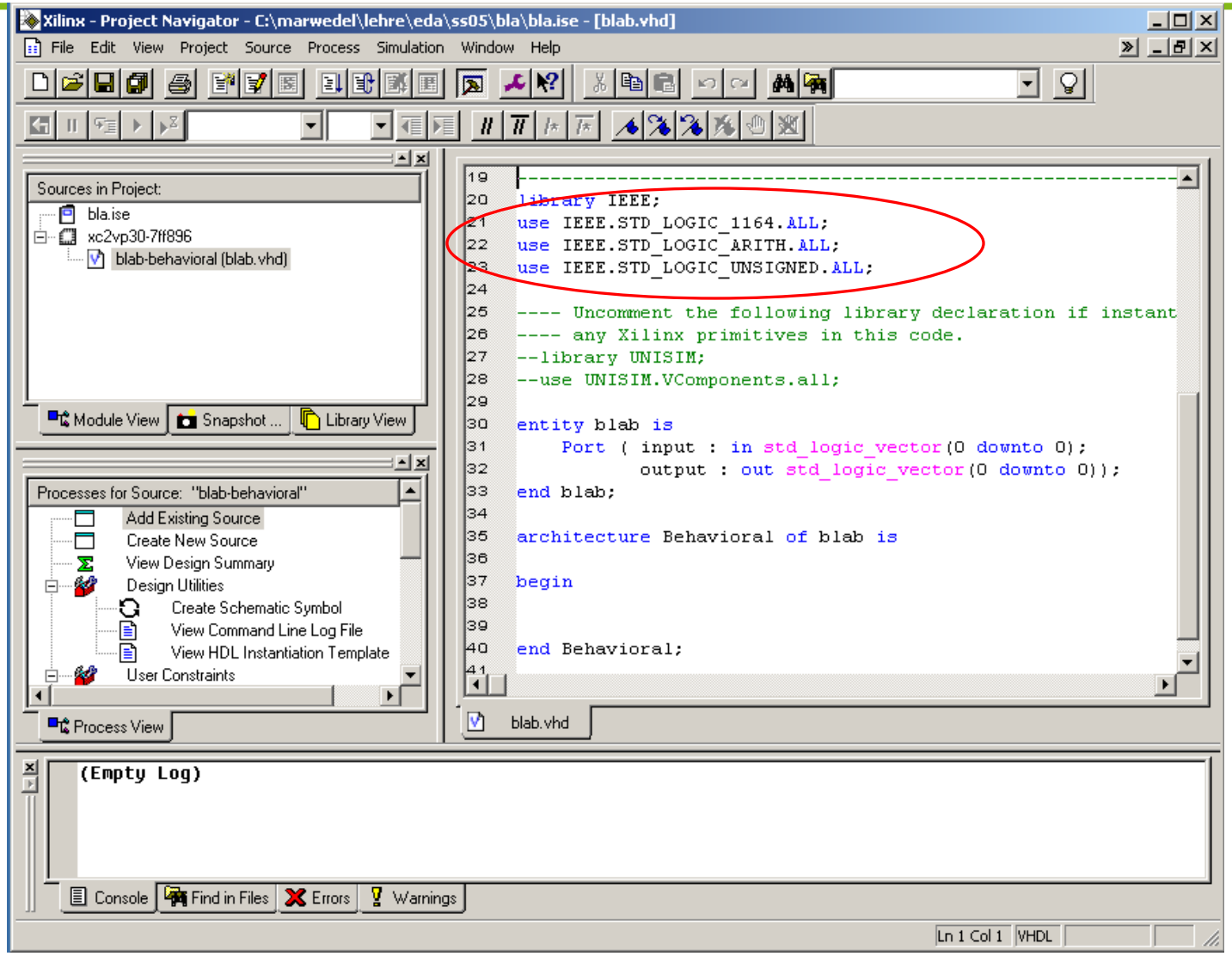
Creating a new VHDL module …



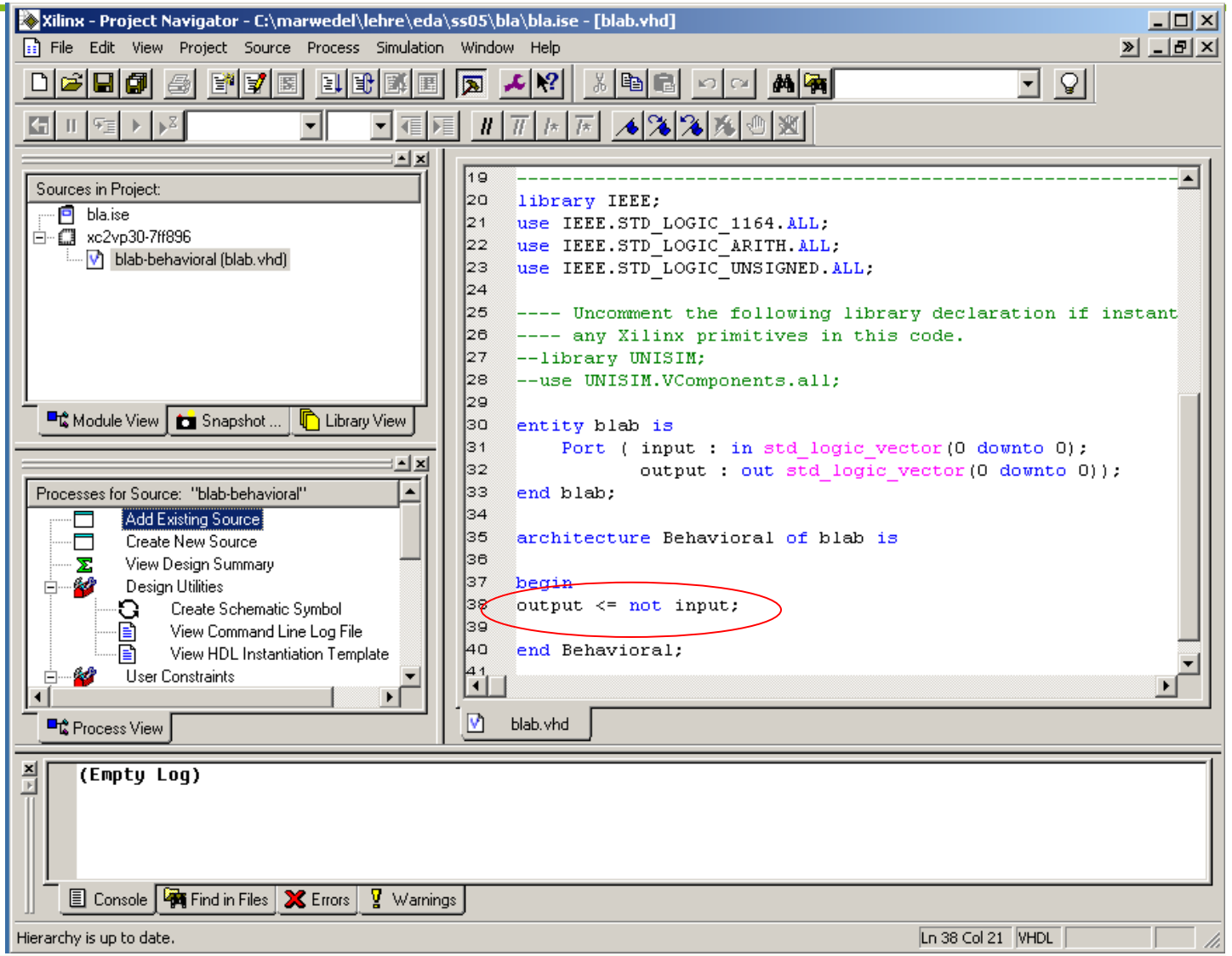
Defining I/O ports



Generated VHDL template

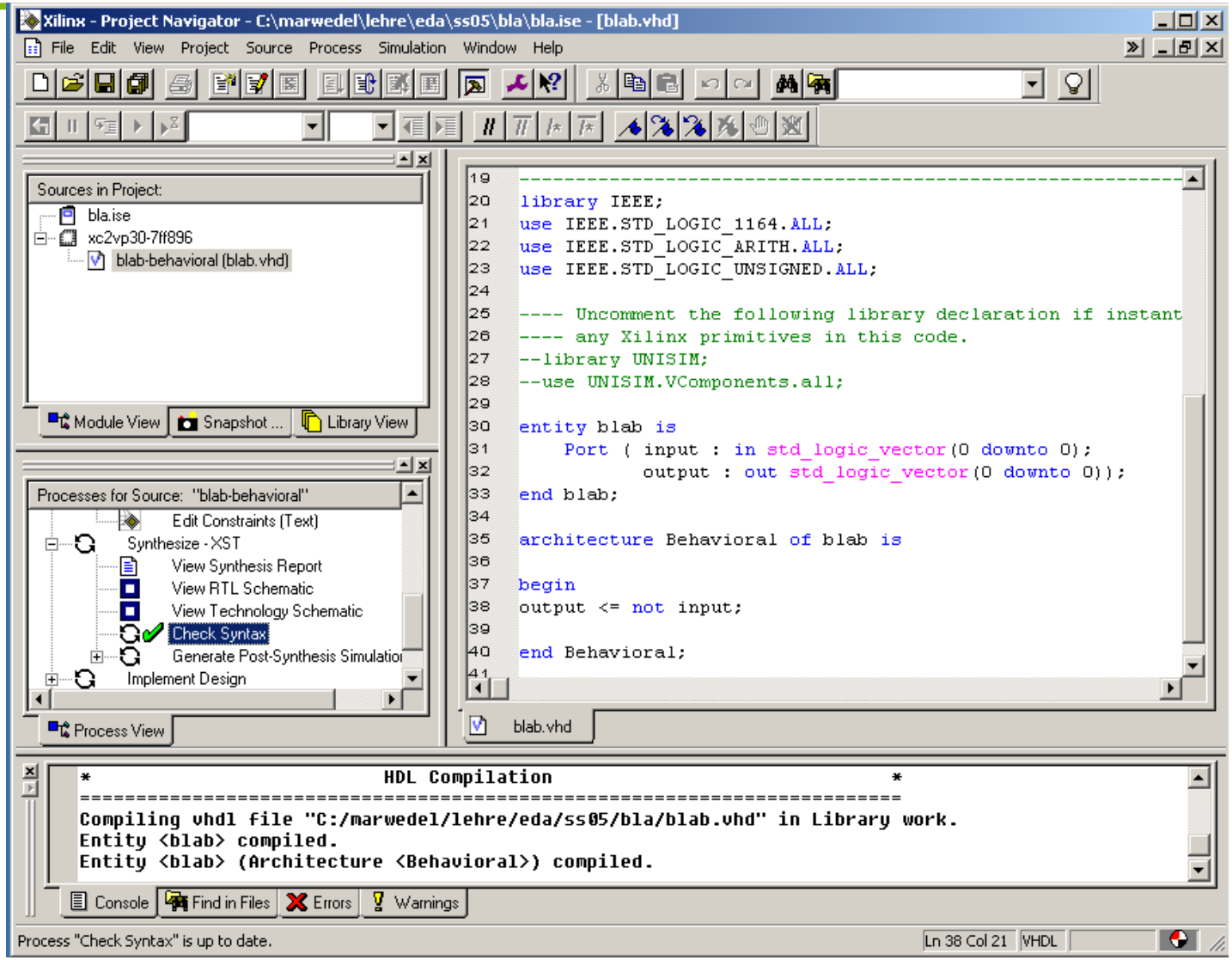


Defining the behavior …



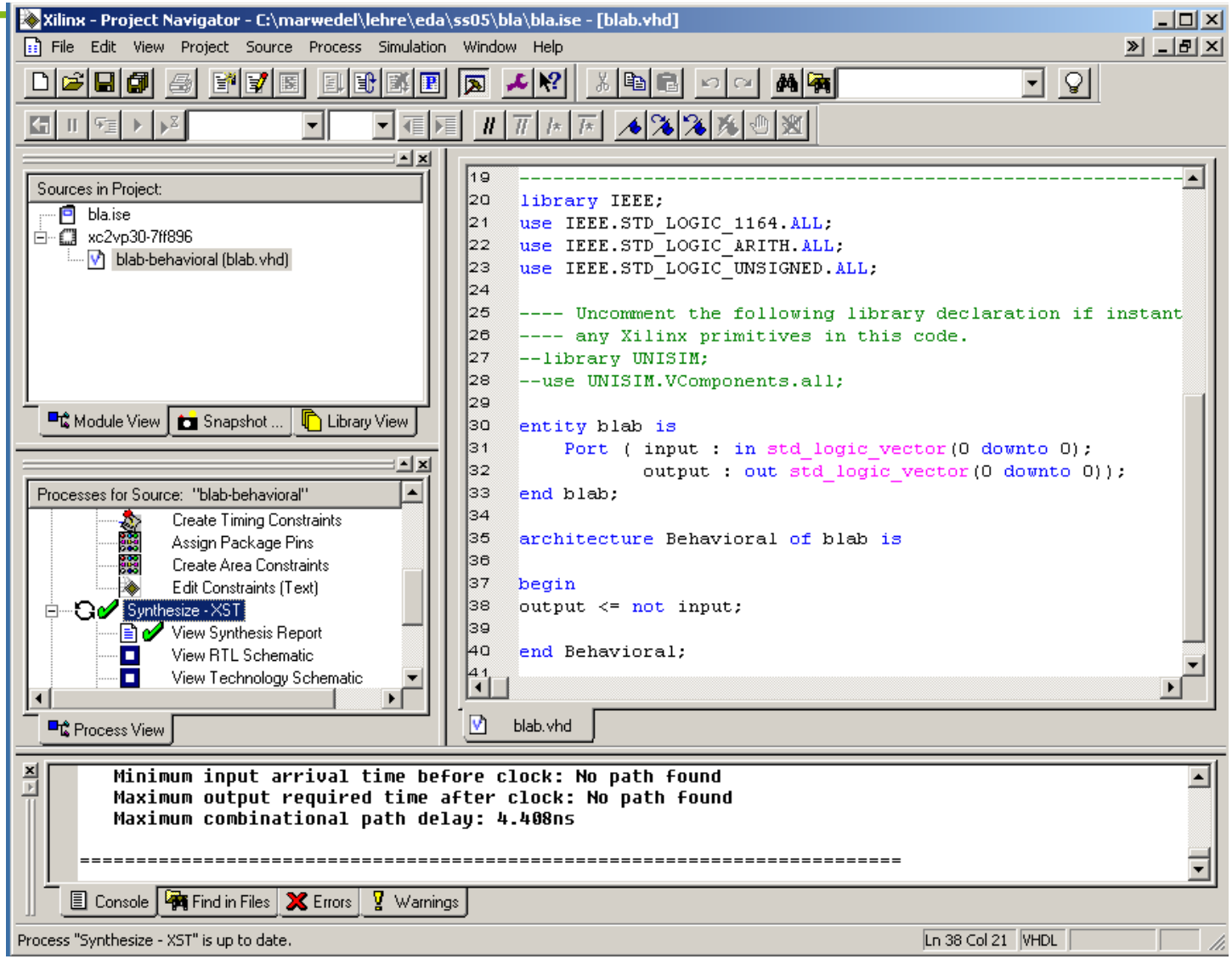
Checking syntax …

Double click on check syntax



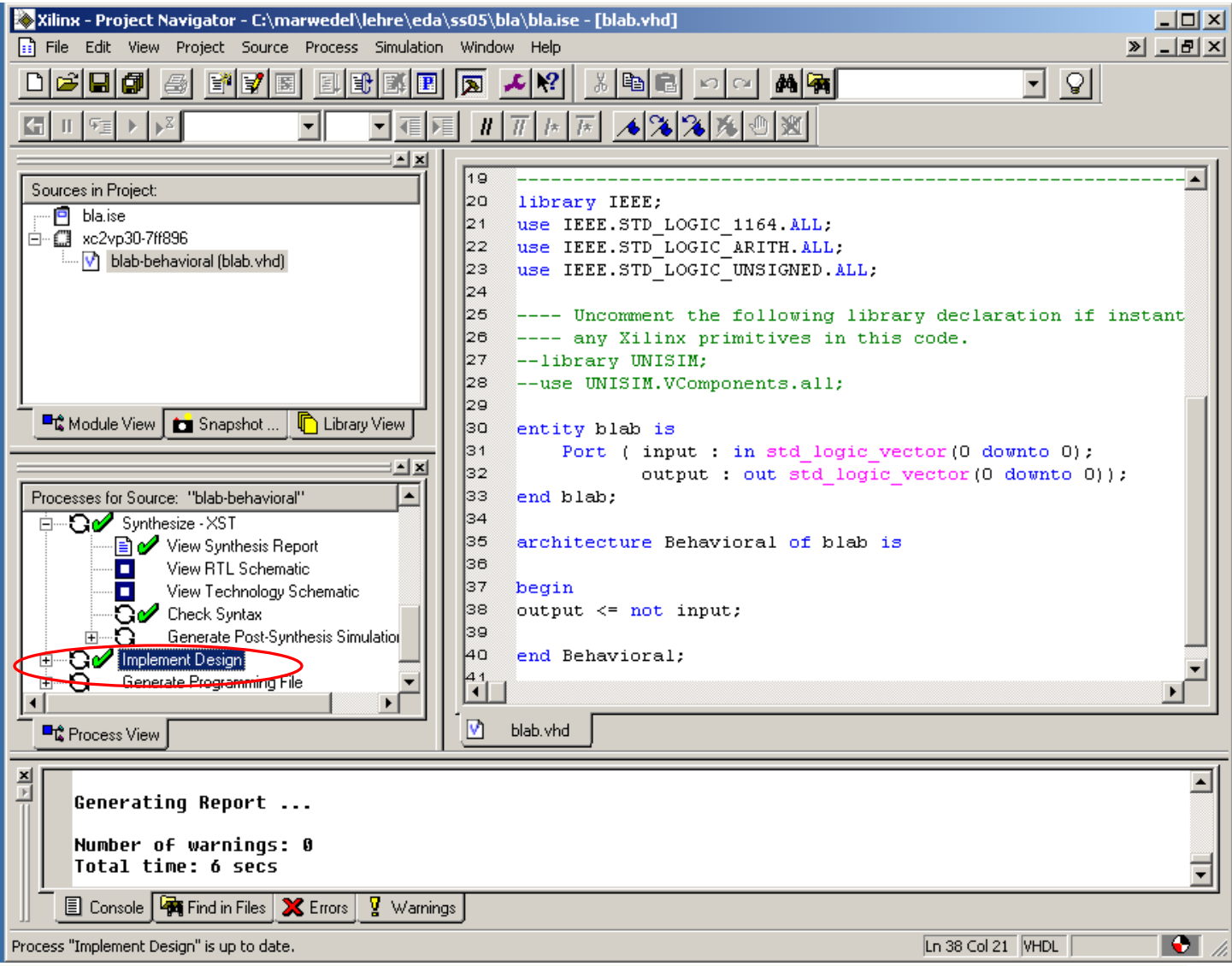
Synthesizing the design …

Double click on synthesize



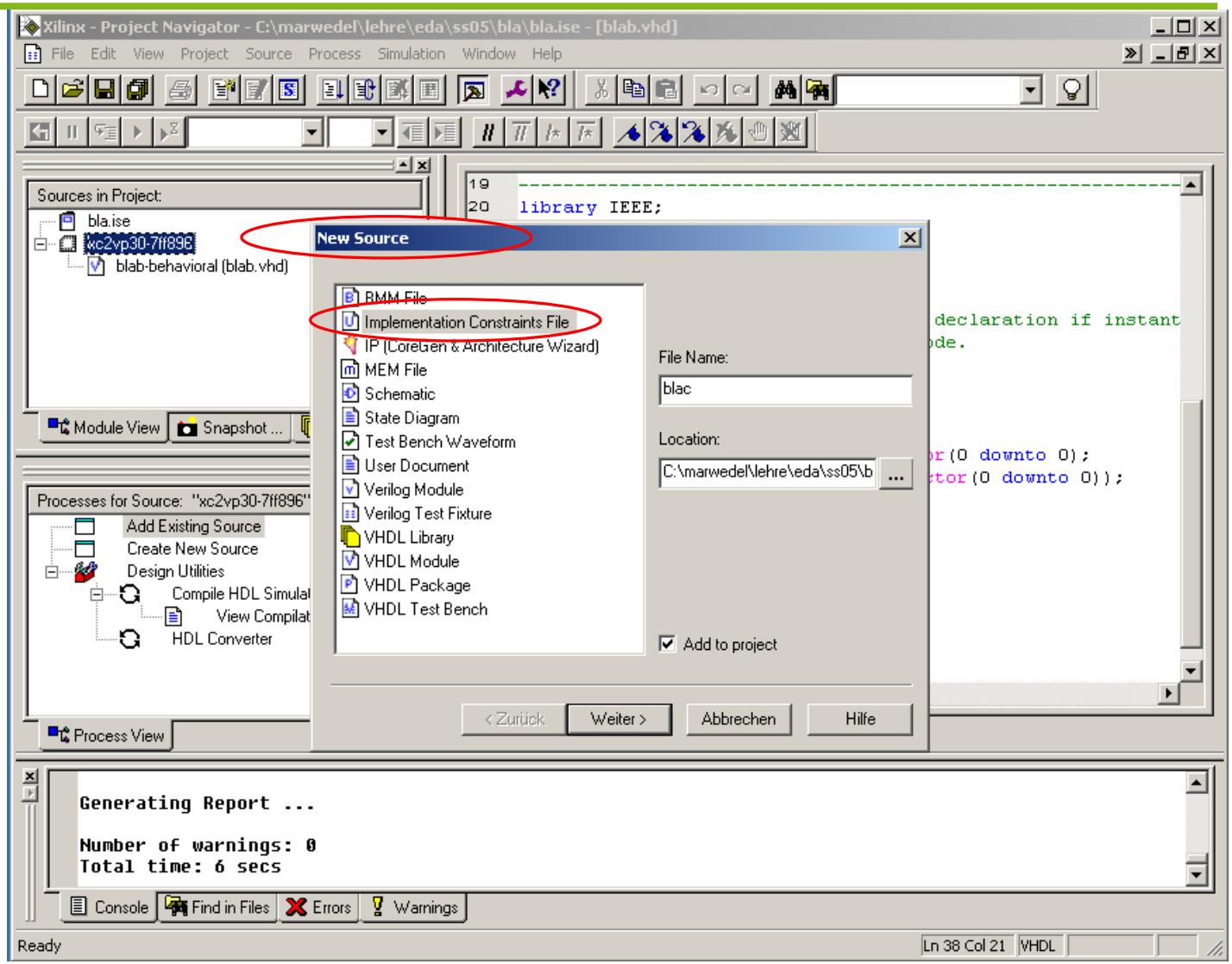
Implementing the design …

Double click on "implement design"

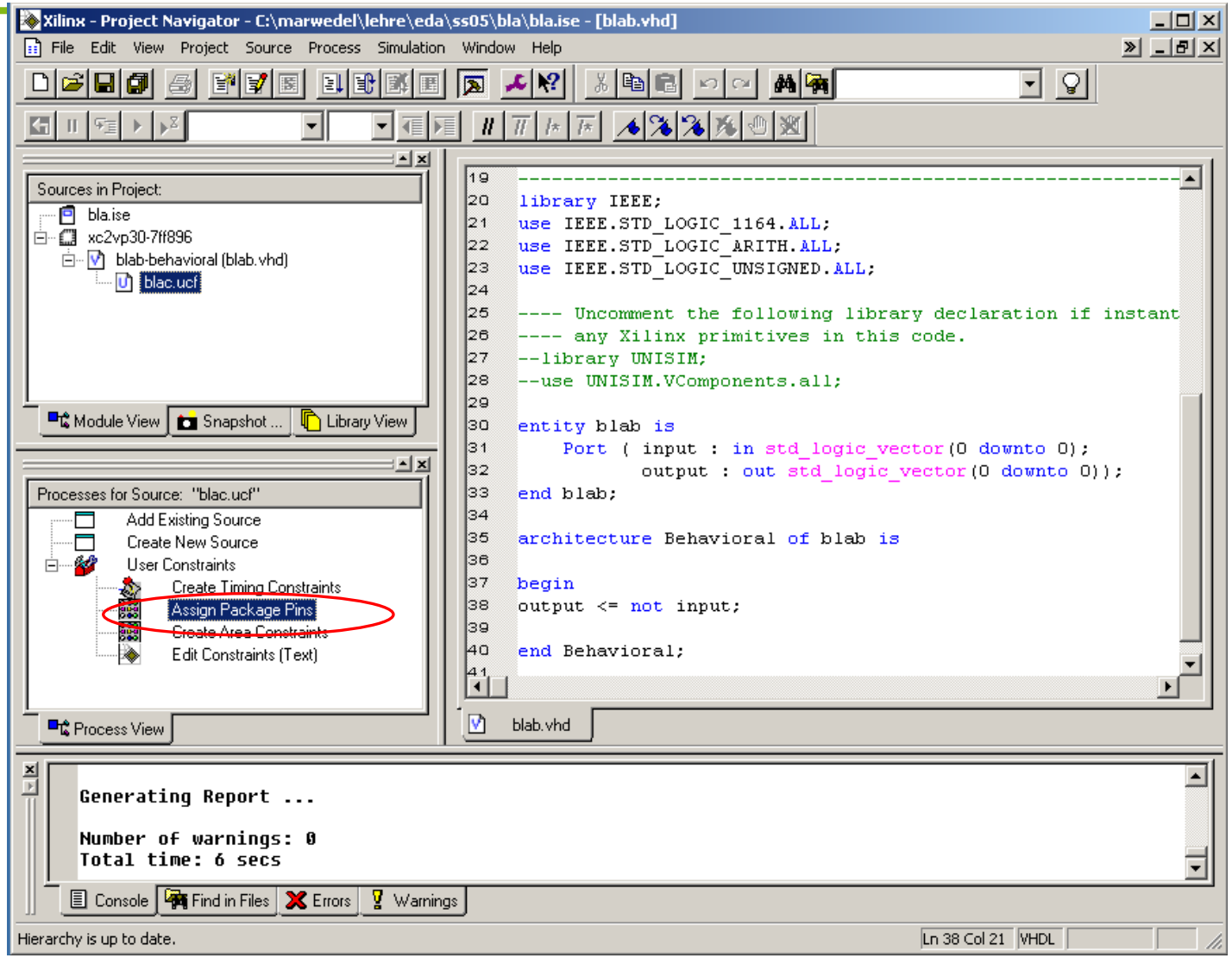


Defining I/O pin constraints …

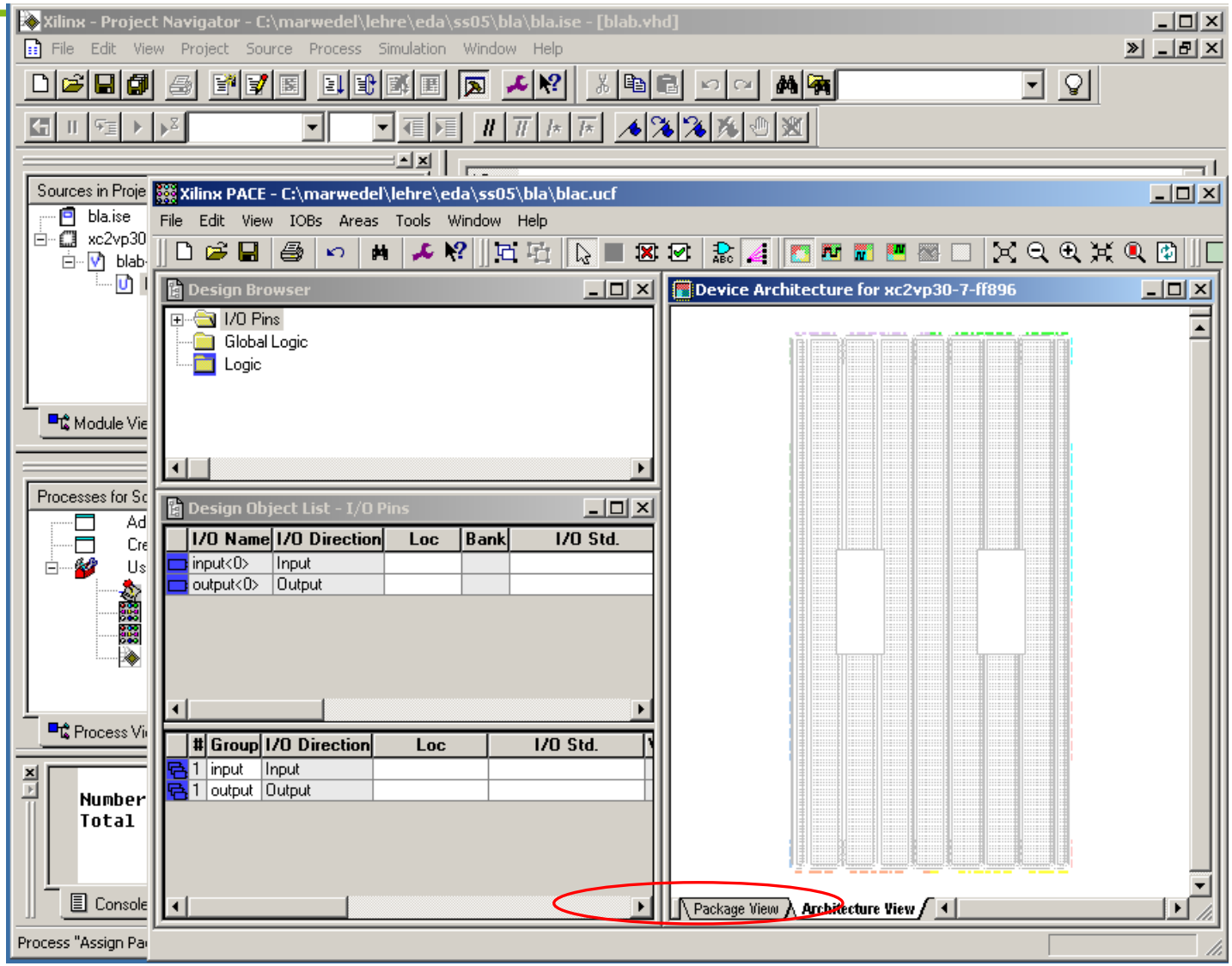
Generate new source and click on implementation constraints



Click on assign package pins

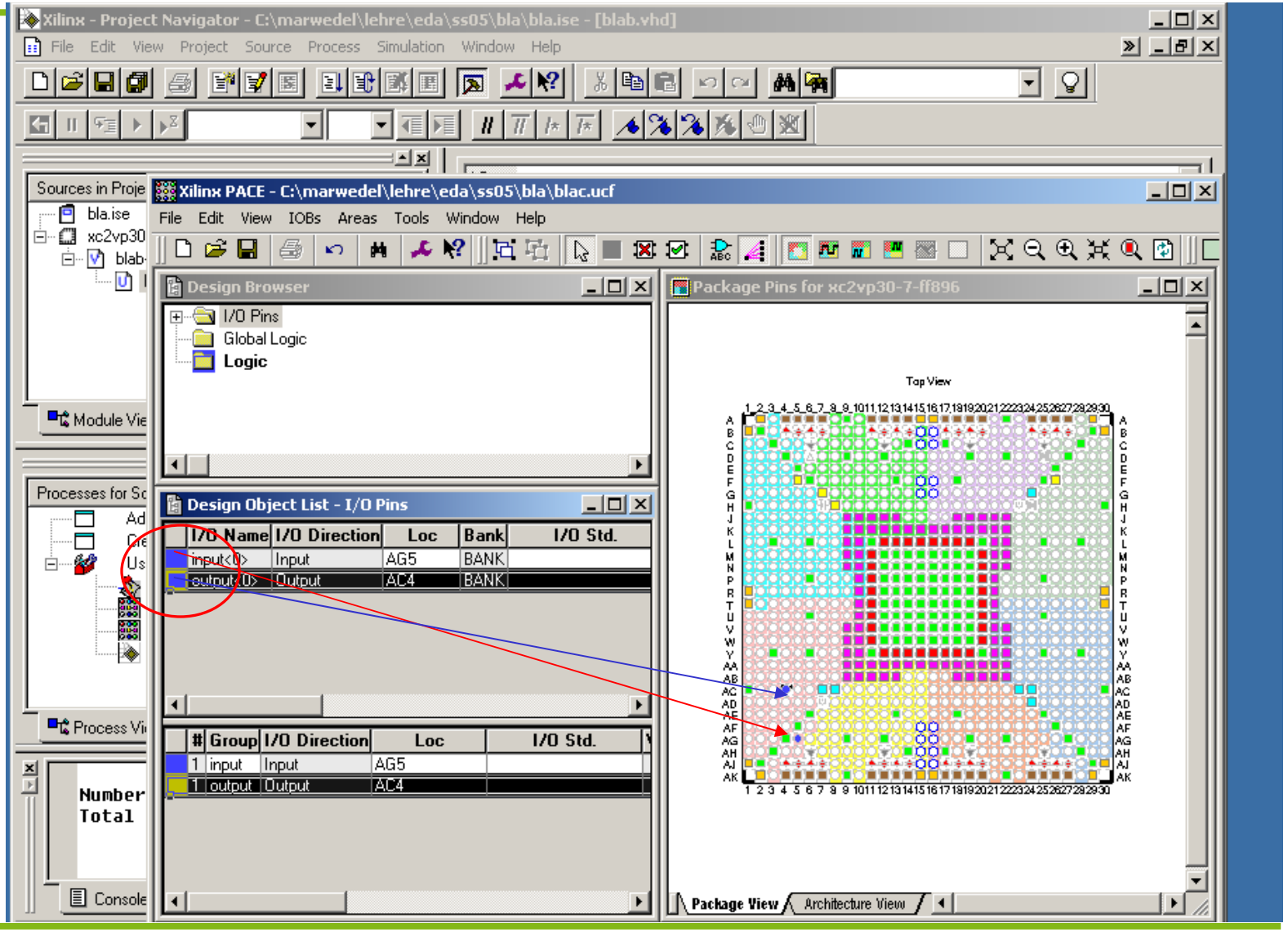


Click on package view

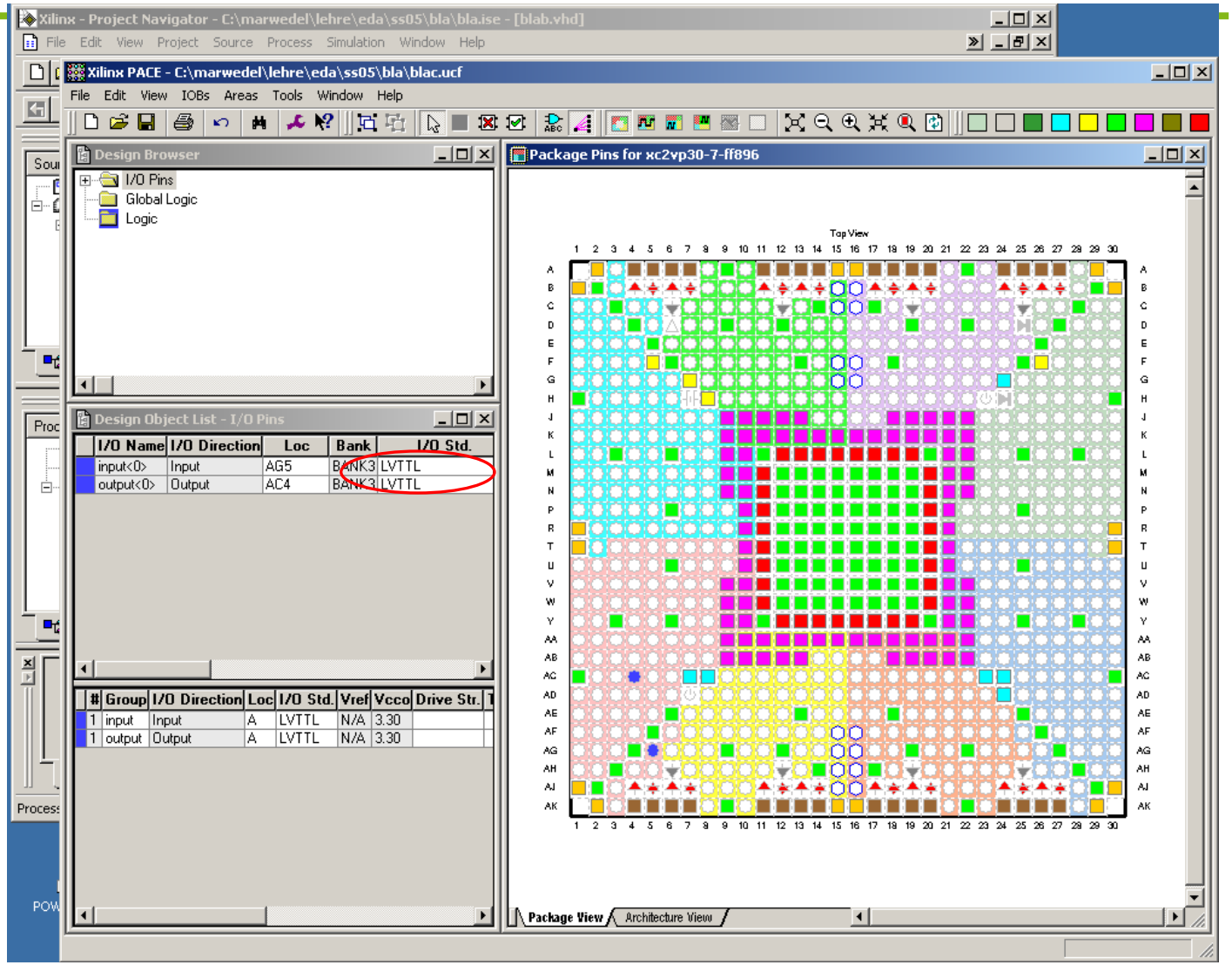


Enter constraints according to list on earlier slide

Drag and drop of box in leftmost column to appro-priate cycle in the layout;



Adjust I/O standard



Summary

- **Our board:**
  XUP V2P board: XCV2P30 FPGA, lots of peripherals.
- **XCV2P30 properties**
  - 80x46 CLBs and
  - Local RAM
  - Multipliers
  - 2 PowerPC processors
- **ISE development software**
  ISE accepts behavioral descriptions in VHDL
  Synthesis and implementation tool steps.
  Pin constraint editor.
  ISE webpack available for everyone free of charge