FPGA Synthesis
Example: Counter

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Gliederung

Zeitplan

- Einführung
- SystemC
  - Vorlesungen und Programmierung

3,5 Wochen

- FPGAs
  - Vorlesungen
  - VHDL-basierte Konfiguration von FPGAs mit dem XUP VII Pro Entwicklungssystem

3,5 Wochen

- Algorithmen
  - Mikroarchitektur-Synthese
  - Automatensynthese
  - Logiksynthese
  - Layoutsynthese

6 Wochen

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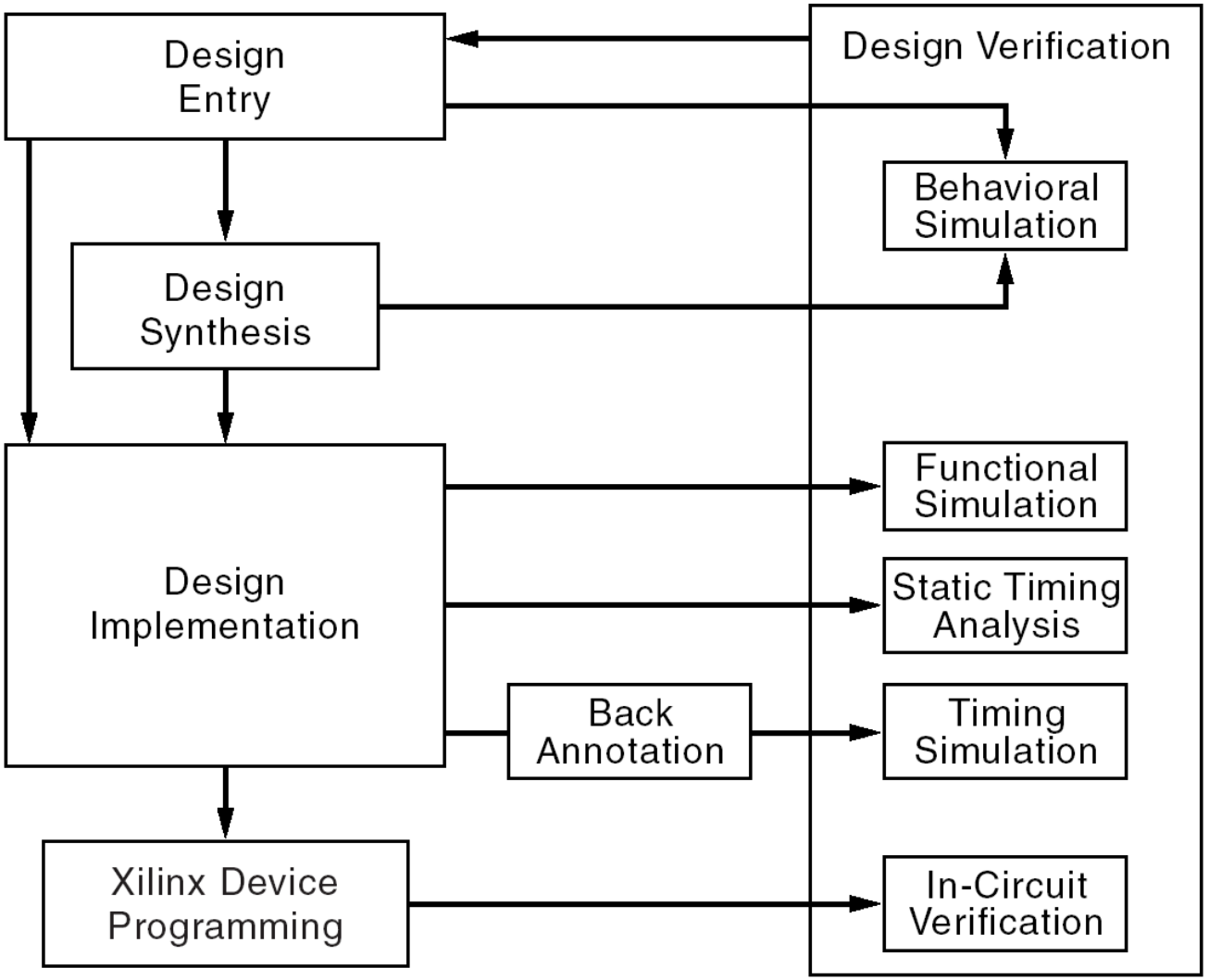
ISE design flow

http://www.xilinx.com/support/sw_manuals/xilinx8/download/qst.zip



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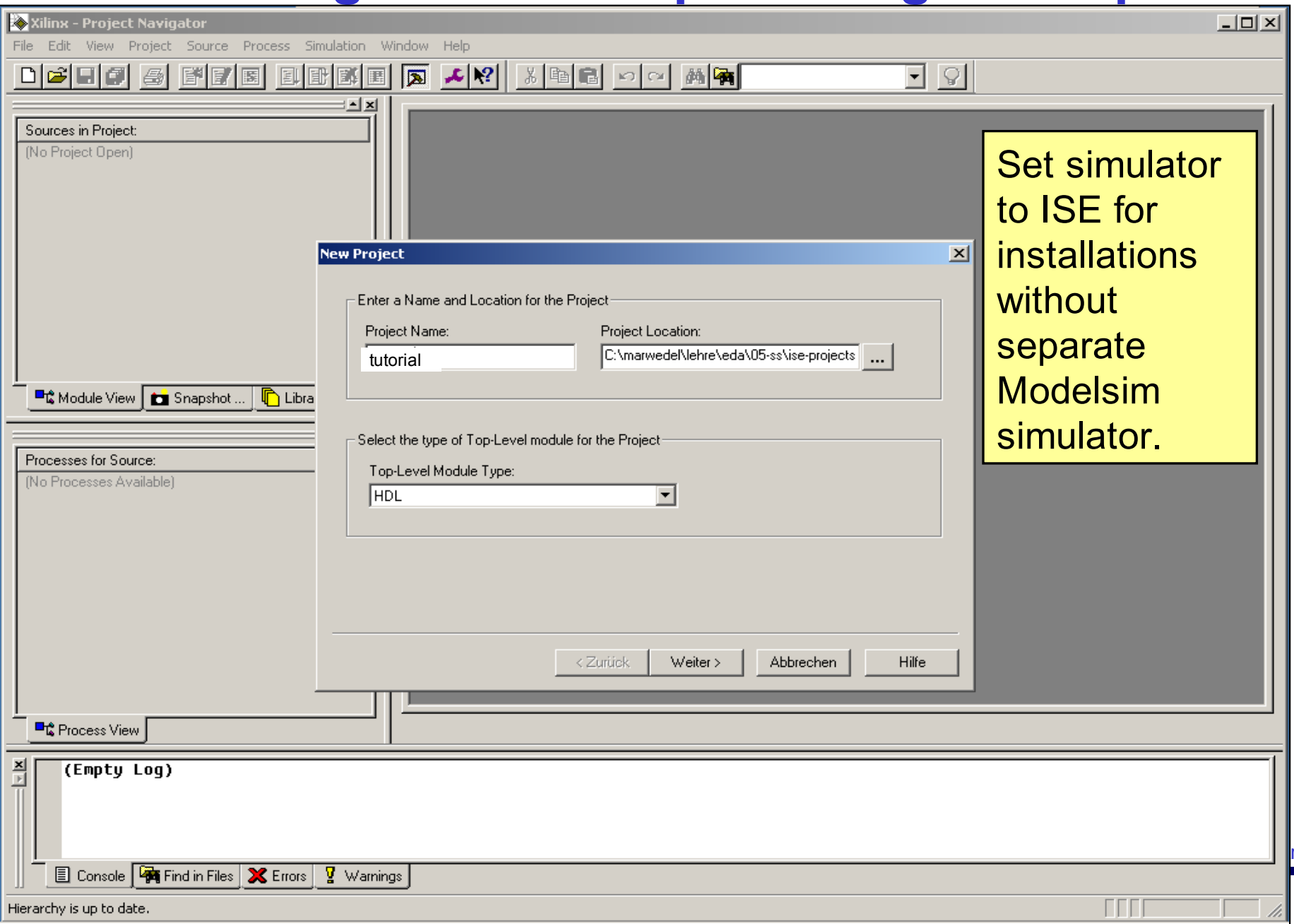
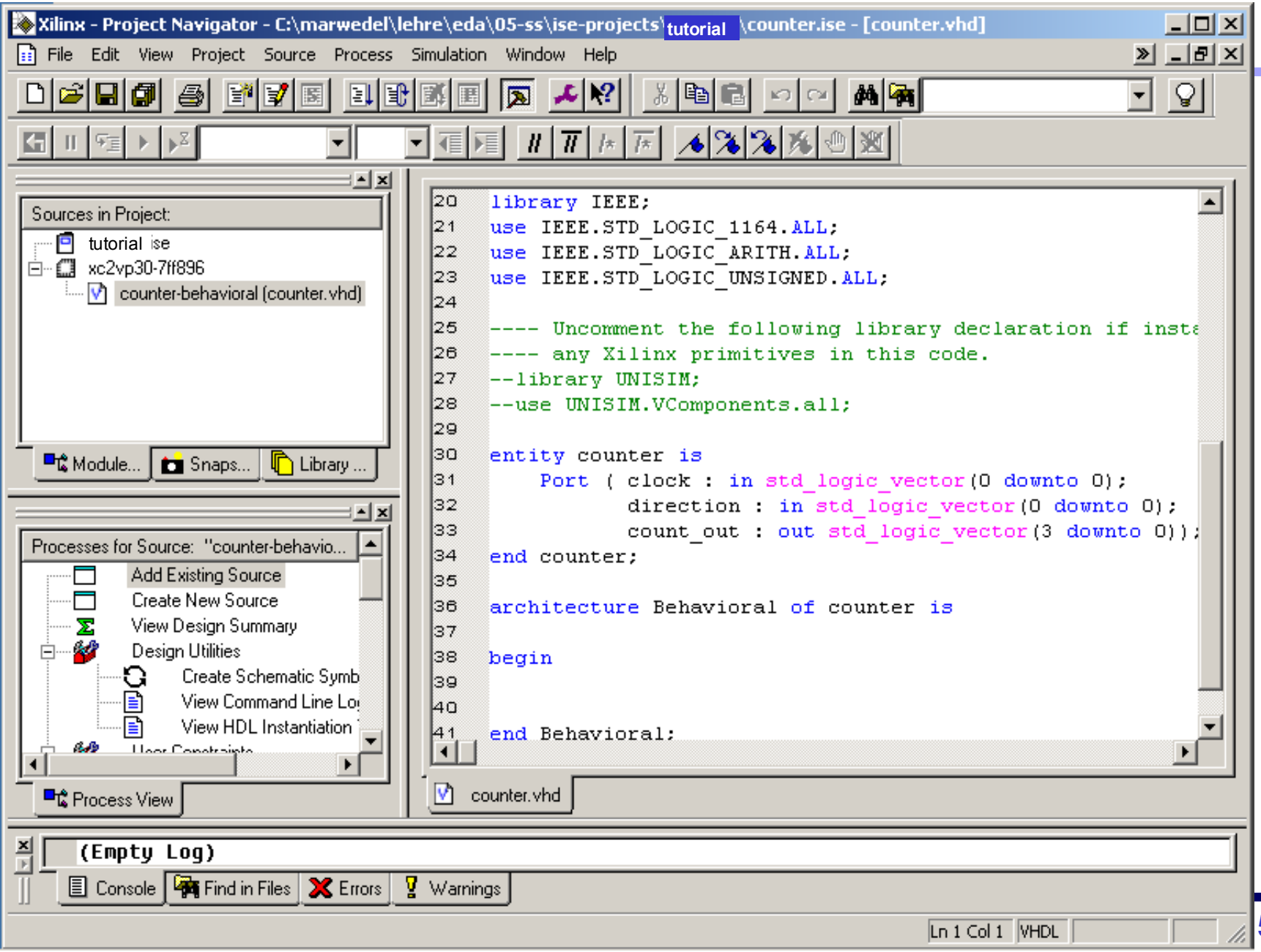
Starting a more complex design example



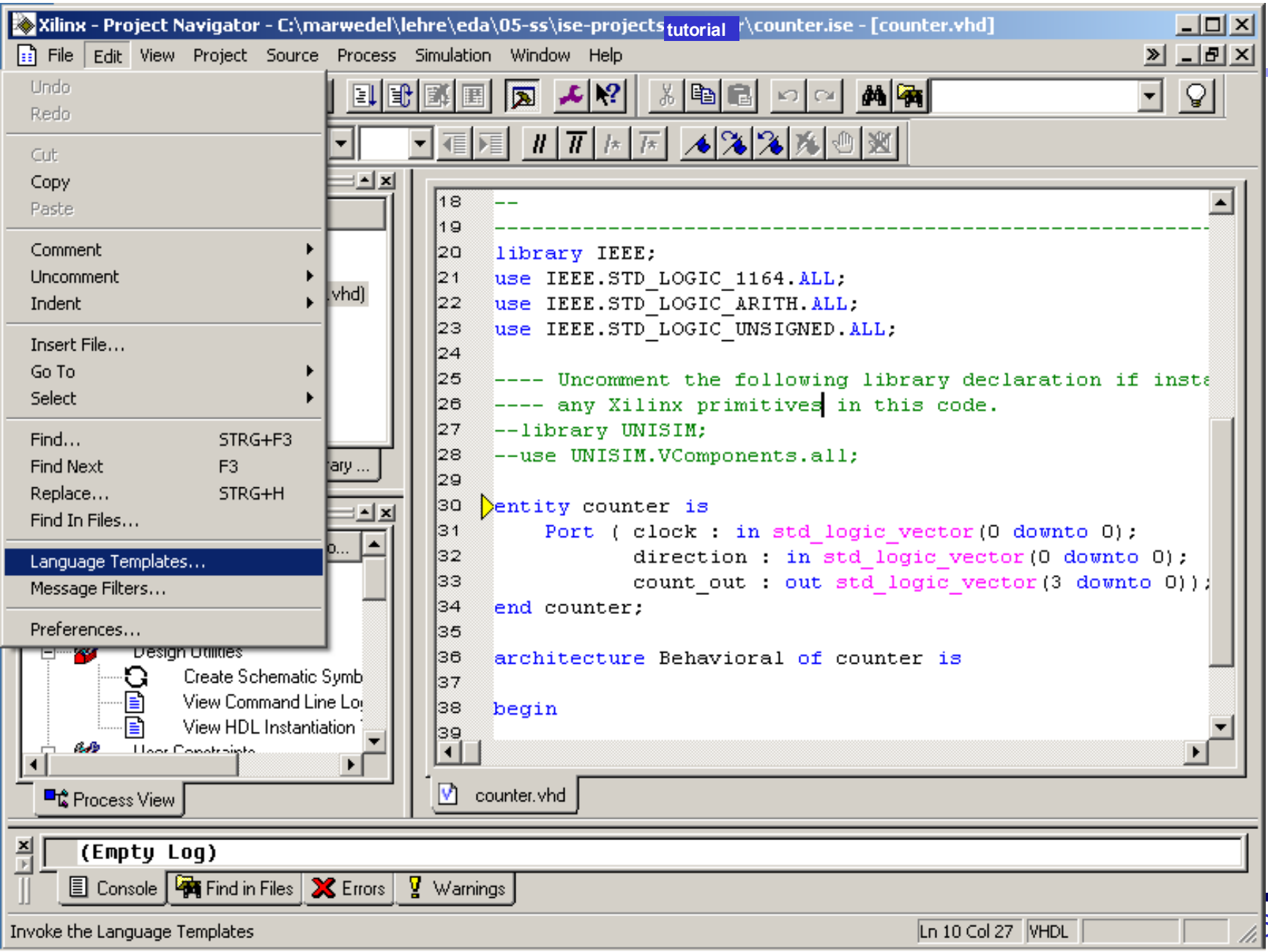
Set simulator to ISE for installations without separate Modelsim simulator.

Some slides use patched project name

Generated design header

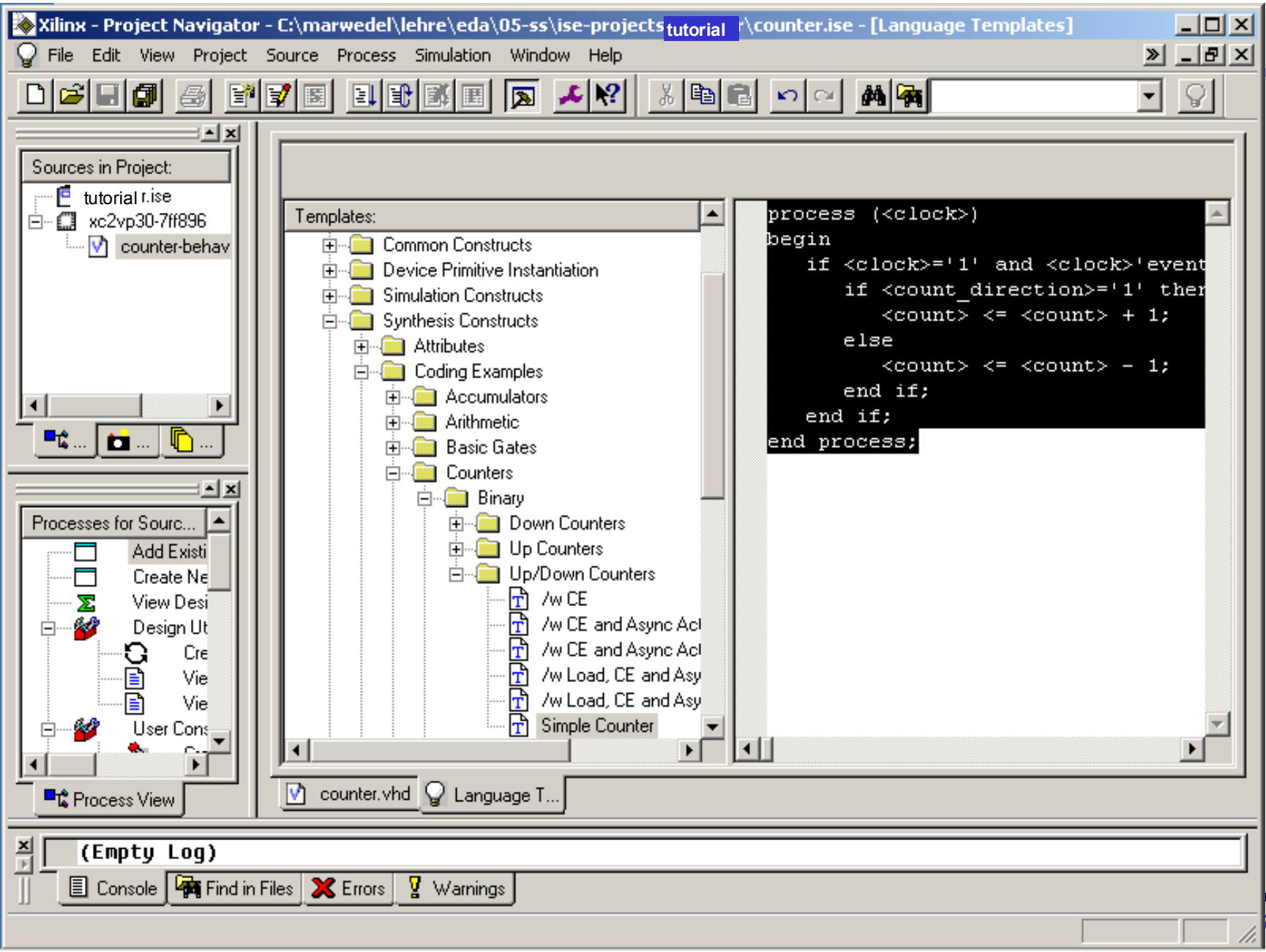


Using language templates to define architectural body



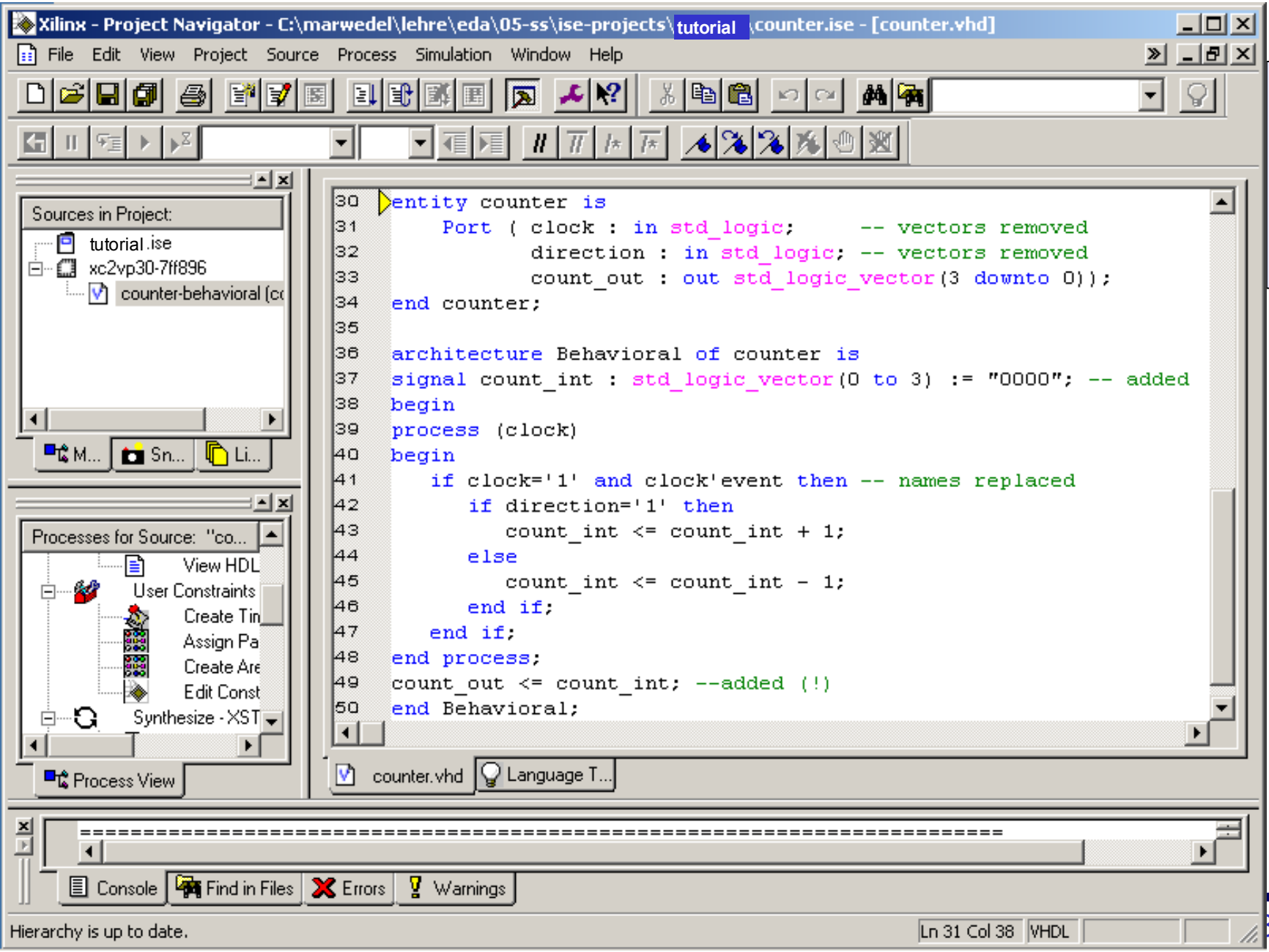
Open edit menu

Select simple counter



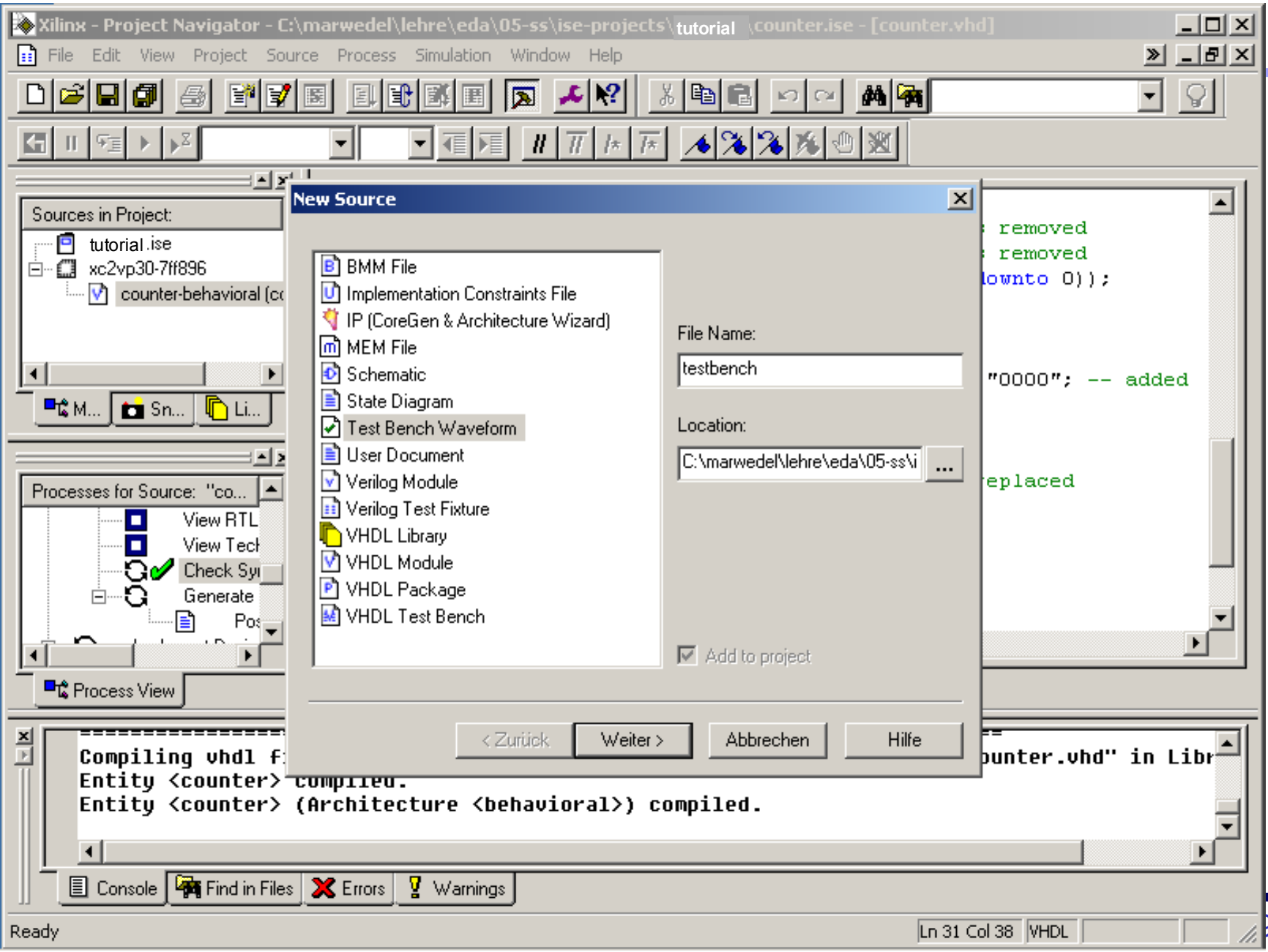
Select simple counter template and copy

Copy template to current design



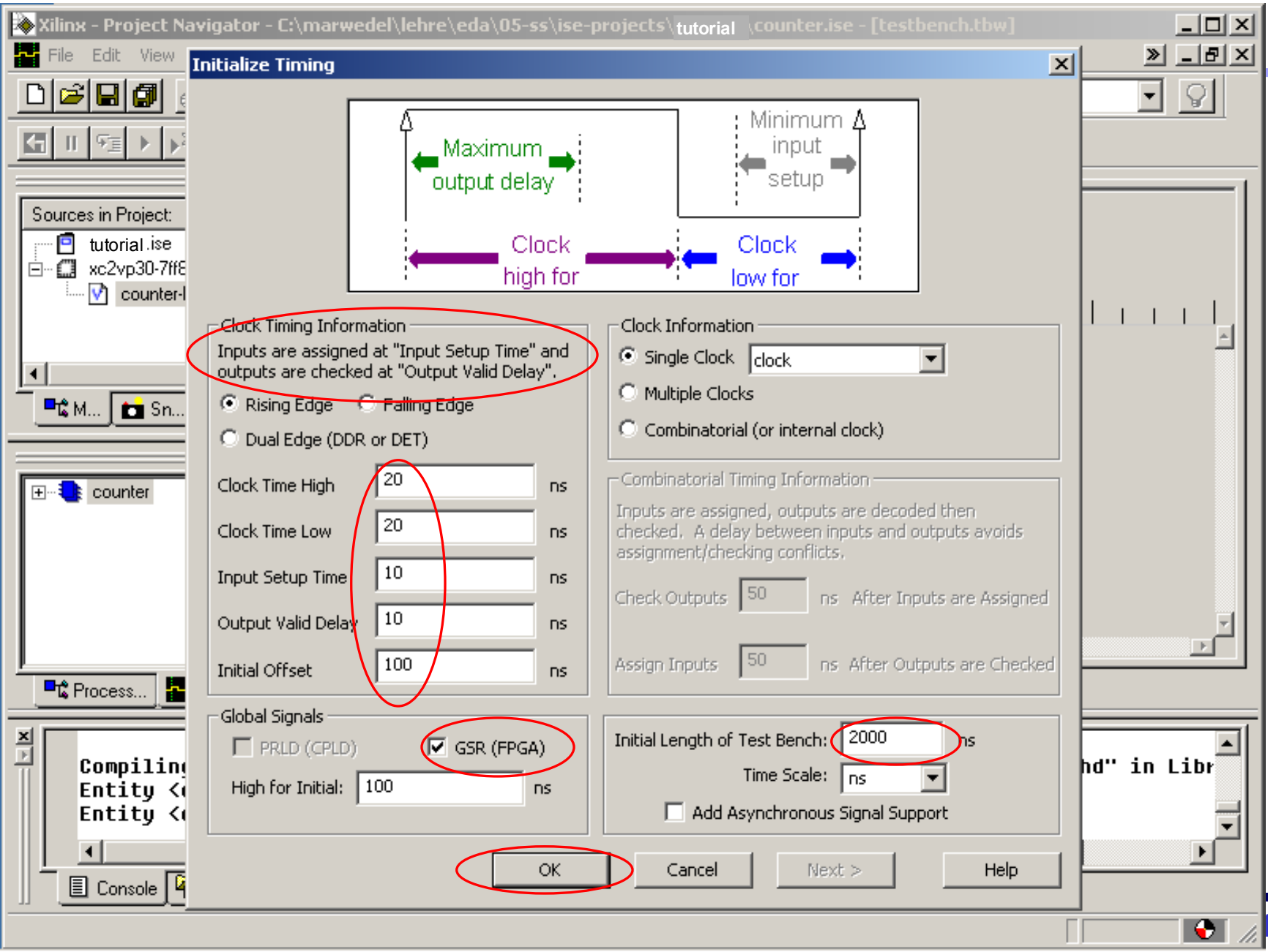
Adapt template as required

Adding testbench

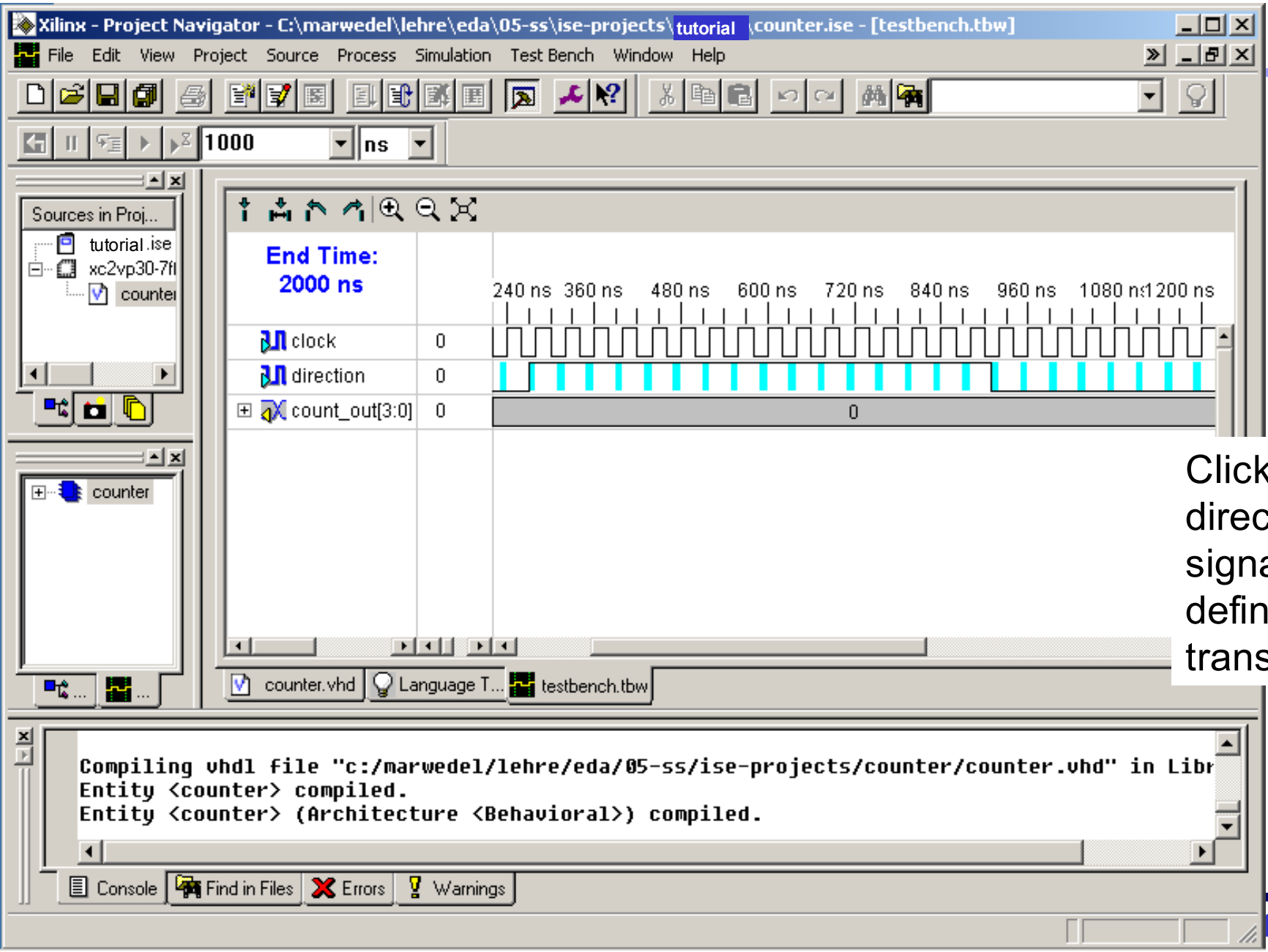


Add new source to counter

Set waveform for clock

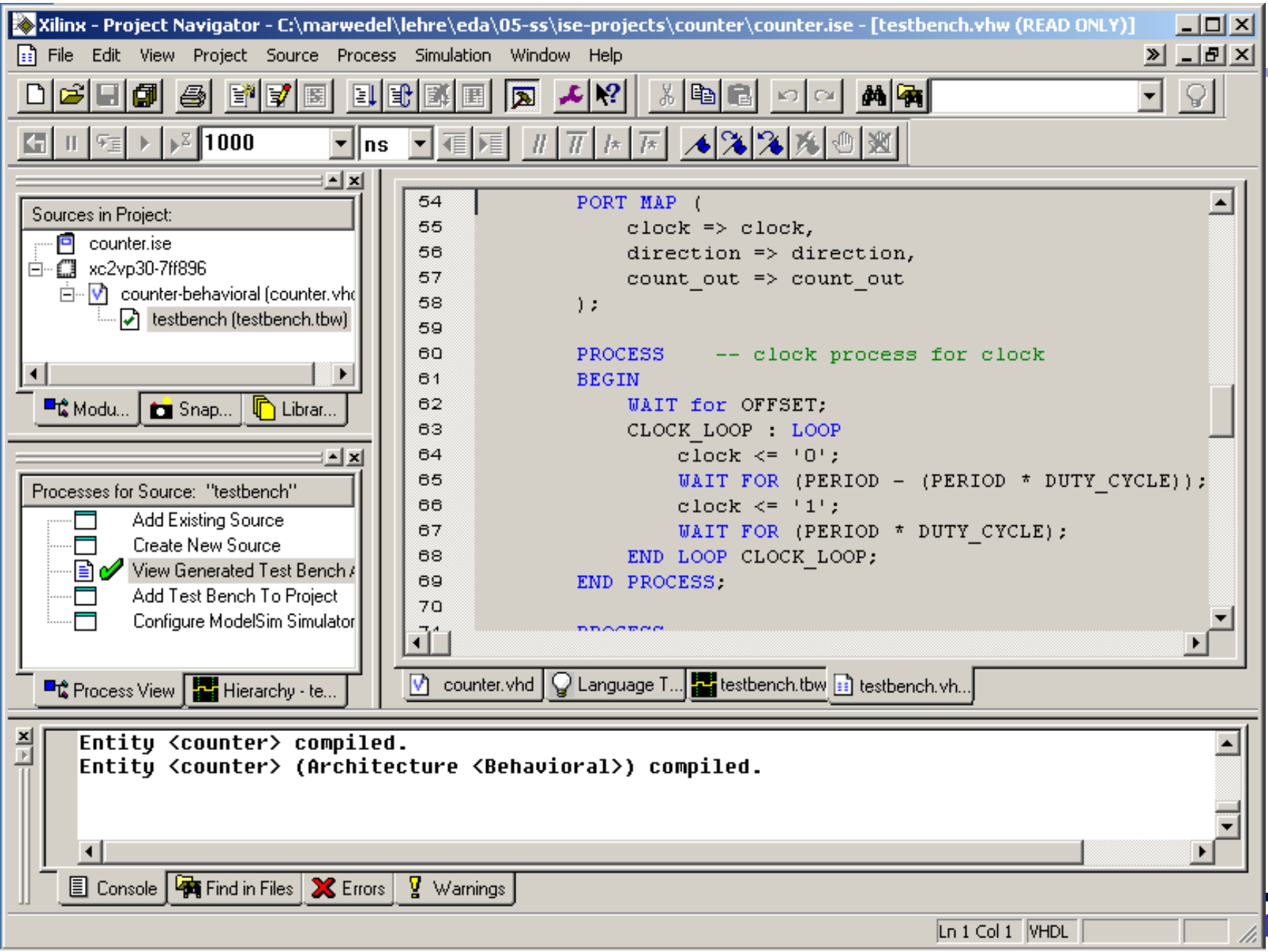


Define waveform for other signals

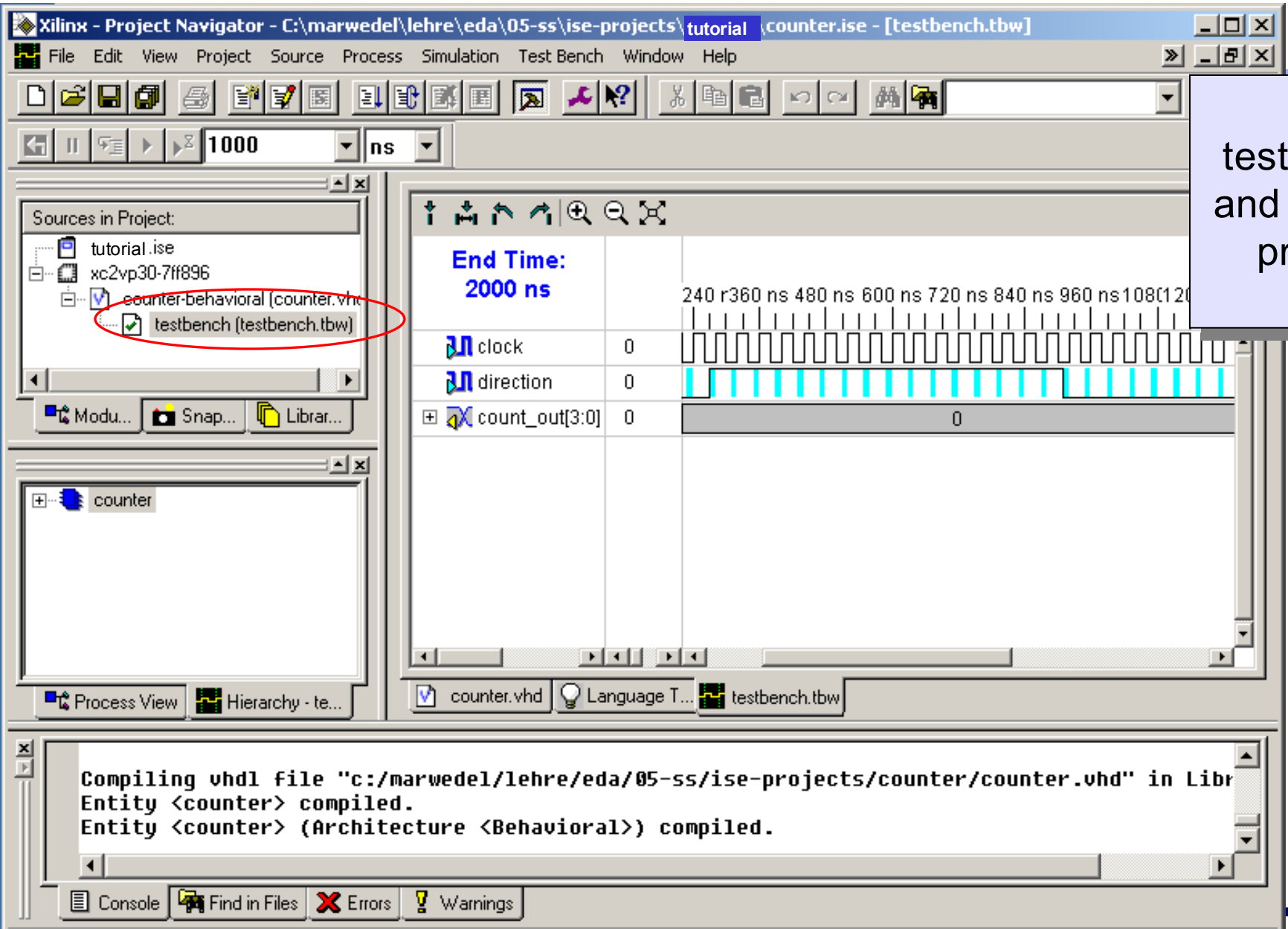


Click on direction signal to define transitions

View generated testbench

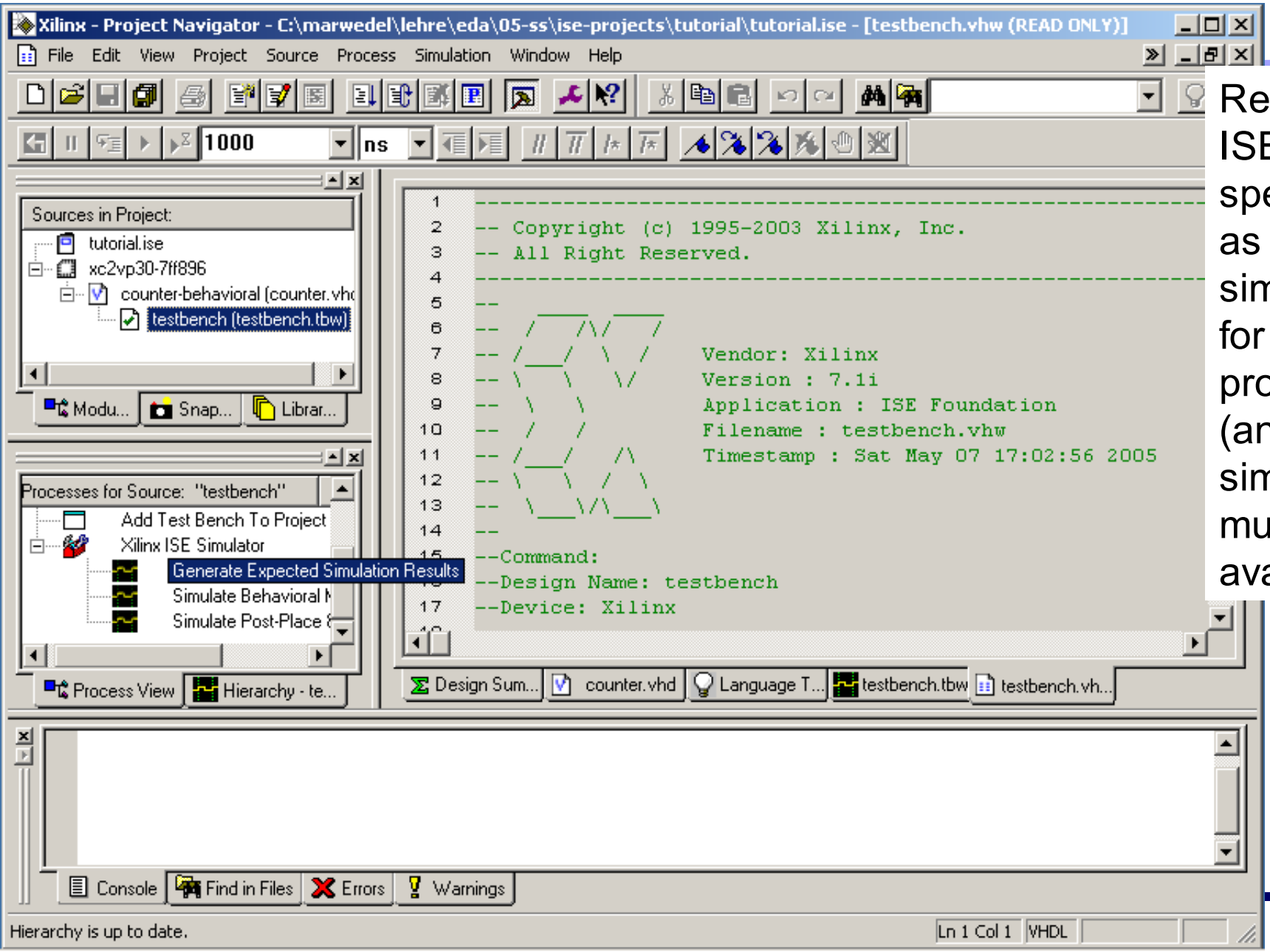


Automatically generate expected waveform (1)



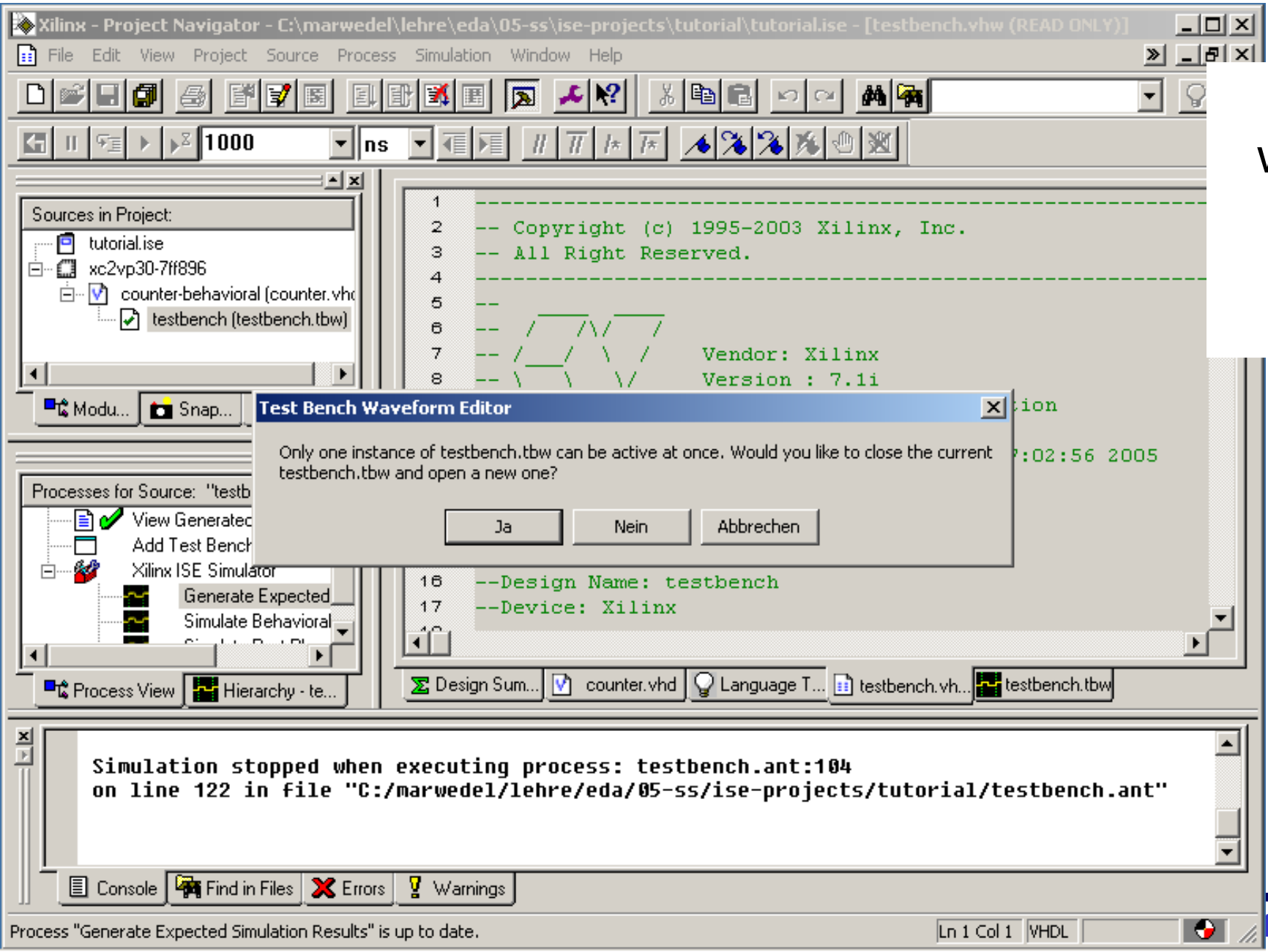
Select testbench and check process view

Automatically generate expected waveform (2)



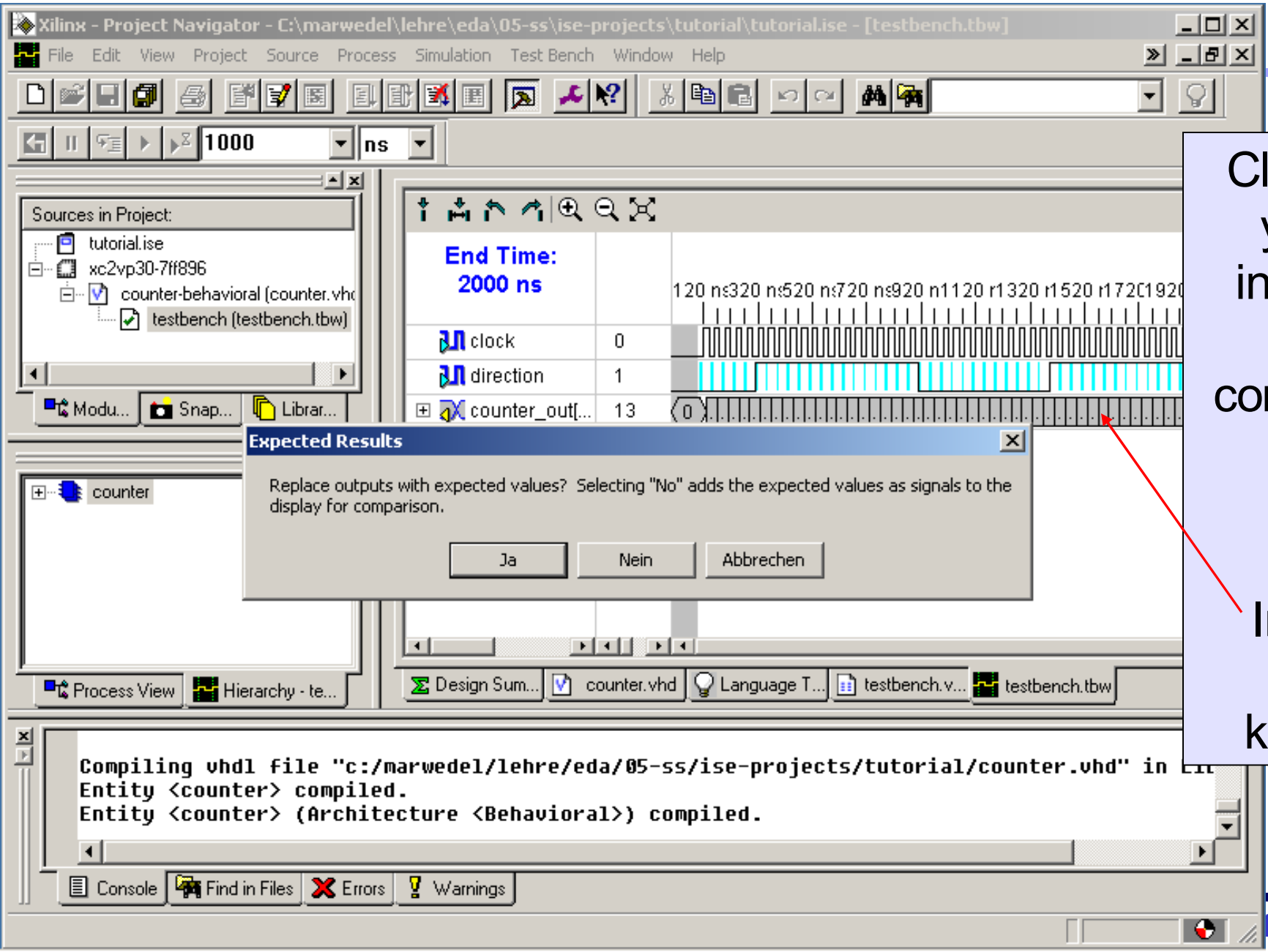
Requires ISE to be specified as the simulator for the project (and simulator must be available).

Replacing the original testbench



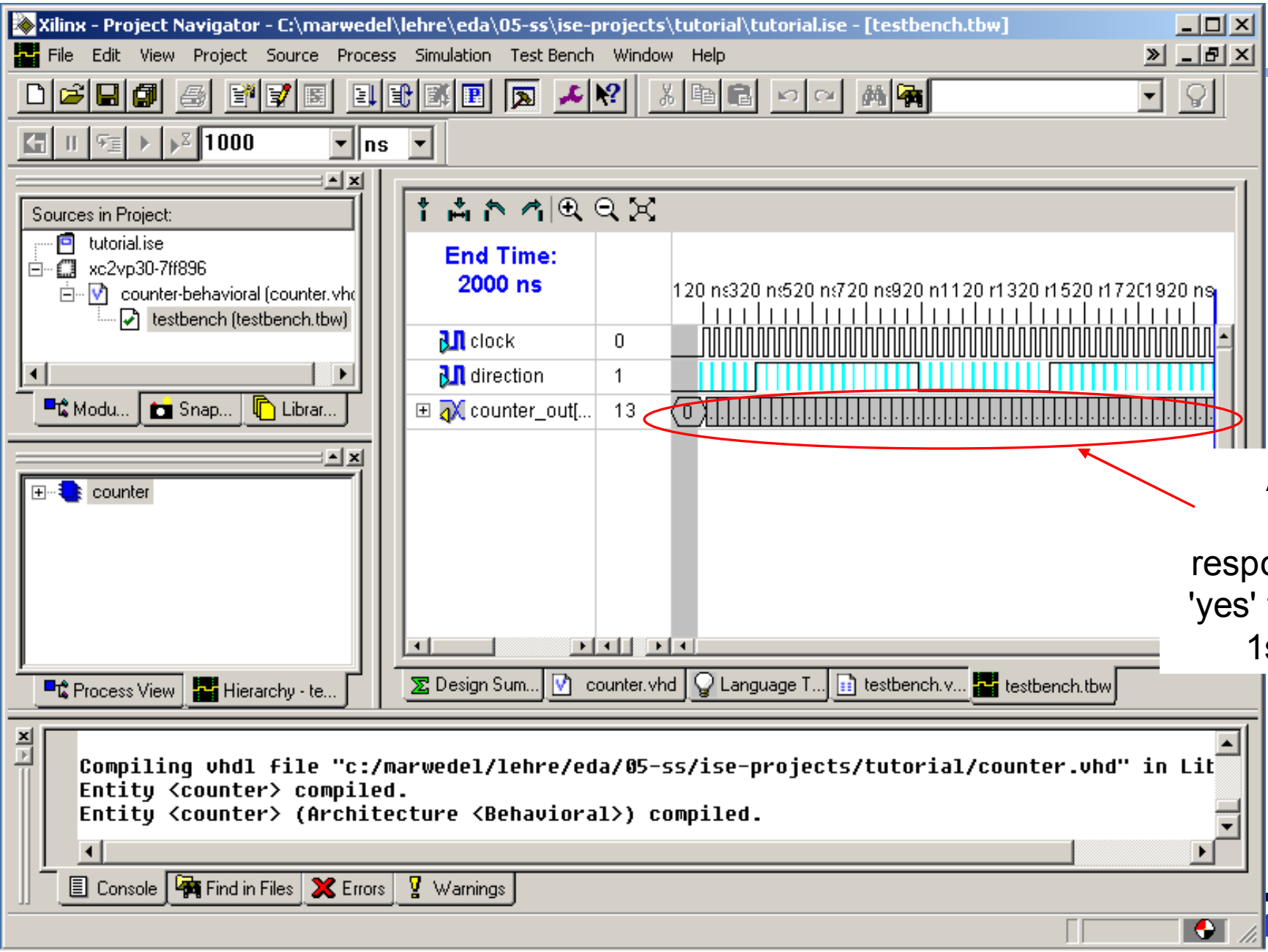
Over-writing initial test-bench

Automatic or manual comparison ?



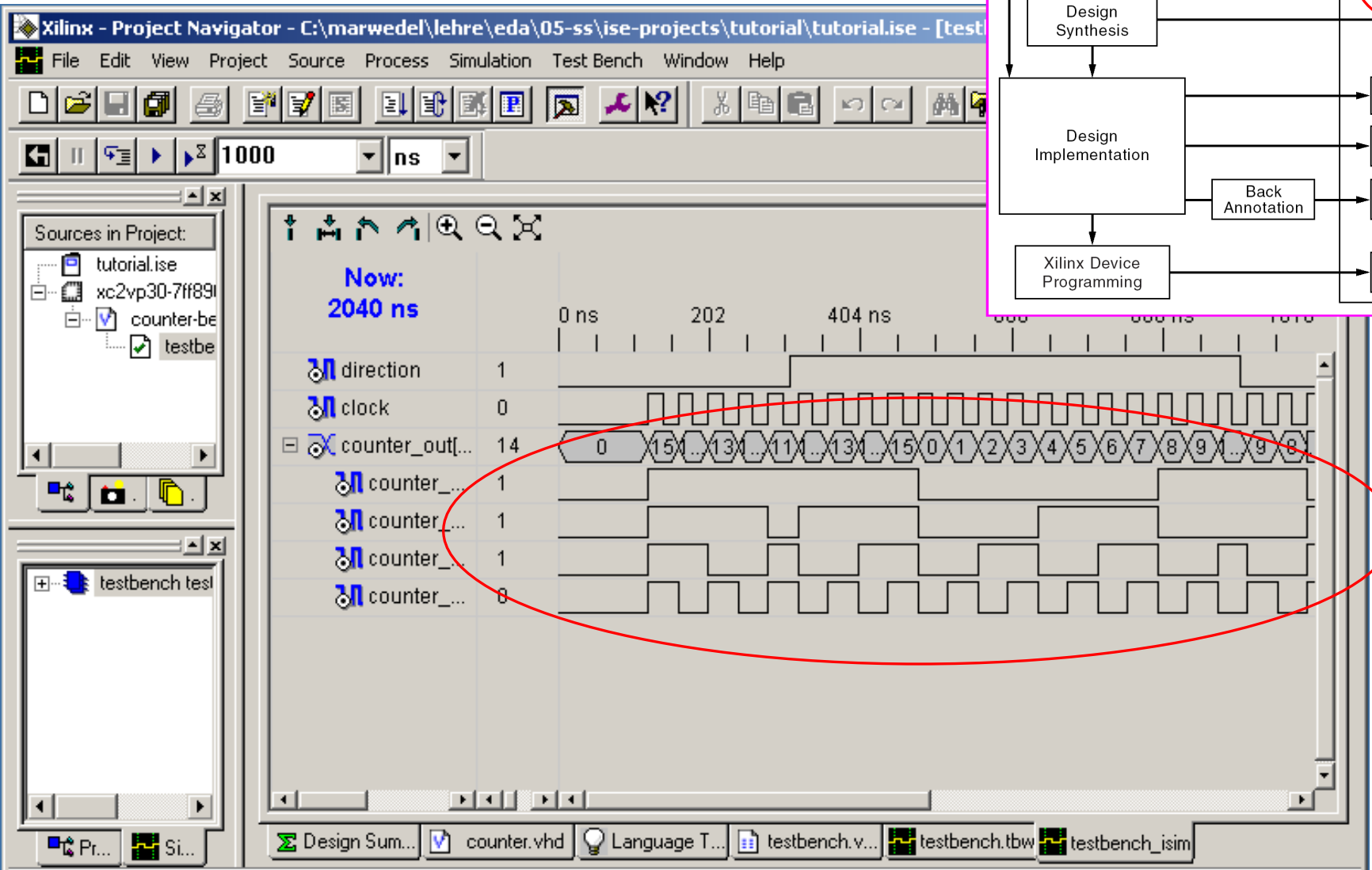
Click on yes/Ja in order to compare auto-mati-cally. Initially un-known.

Automatic comparison

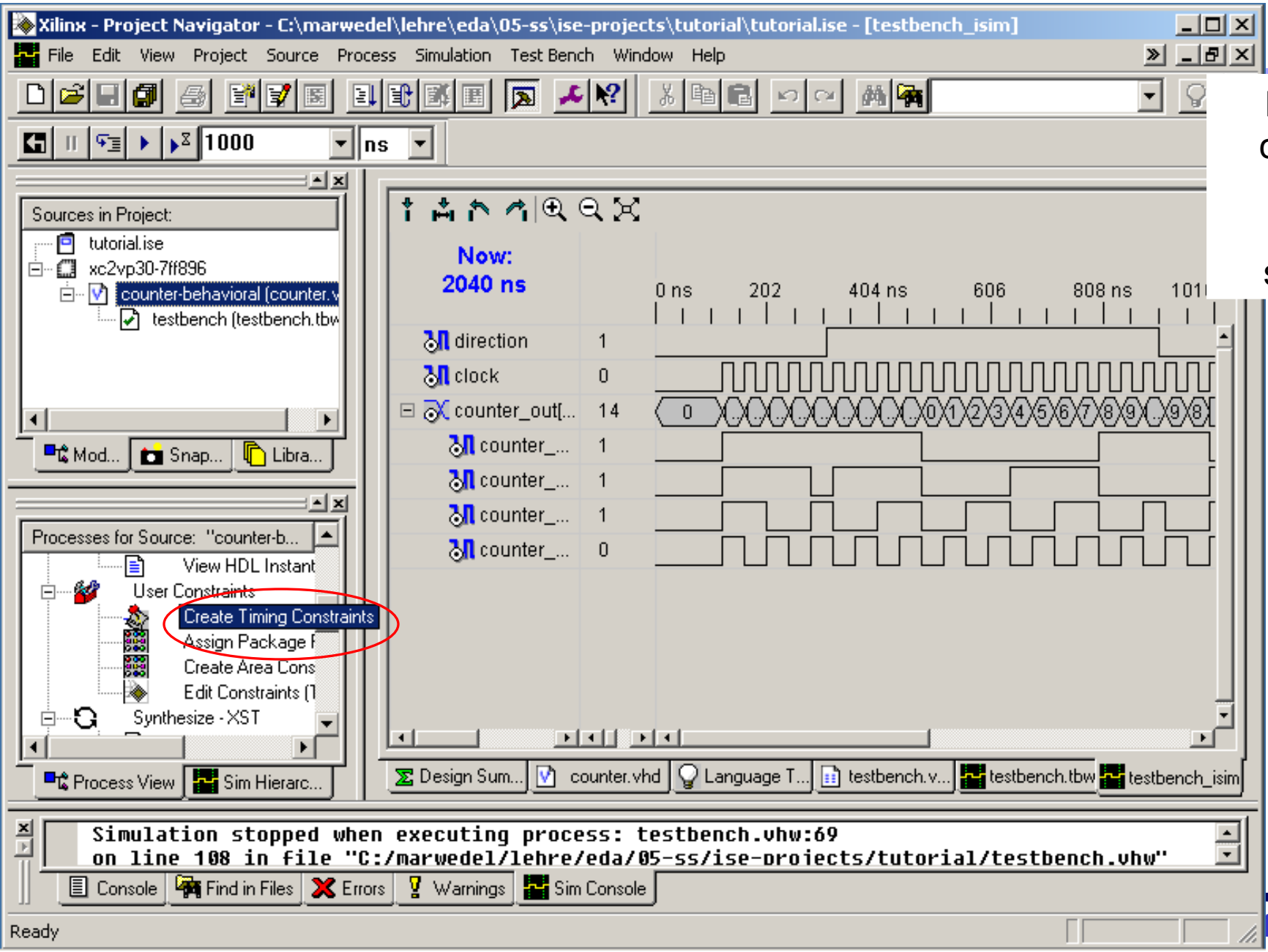


Added when responding 'yes' for the 1st time

Behavioral simulation

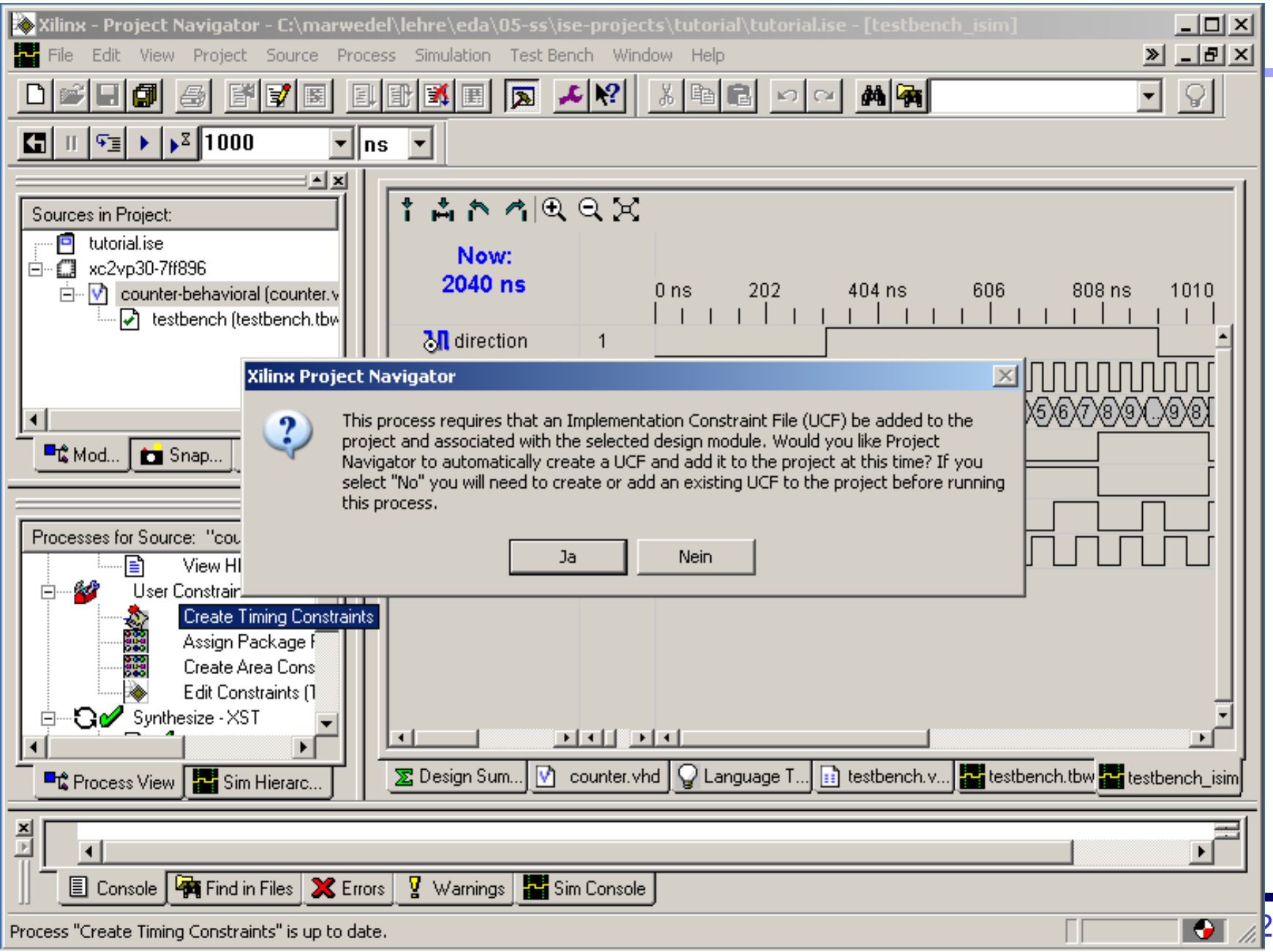


Adding timing constraints (1)

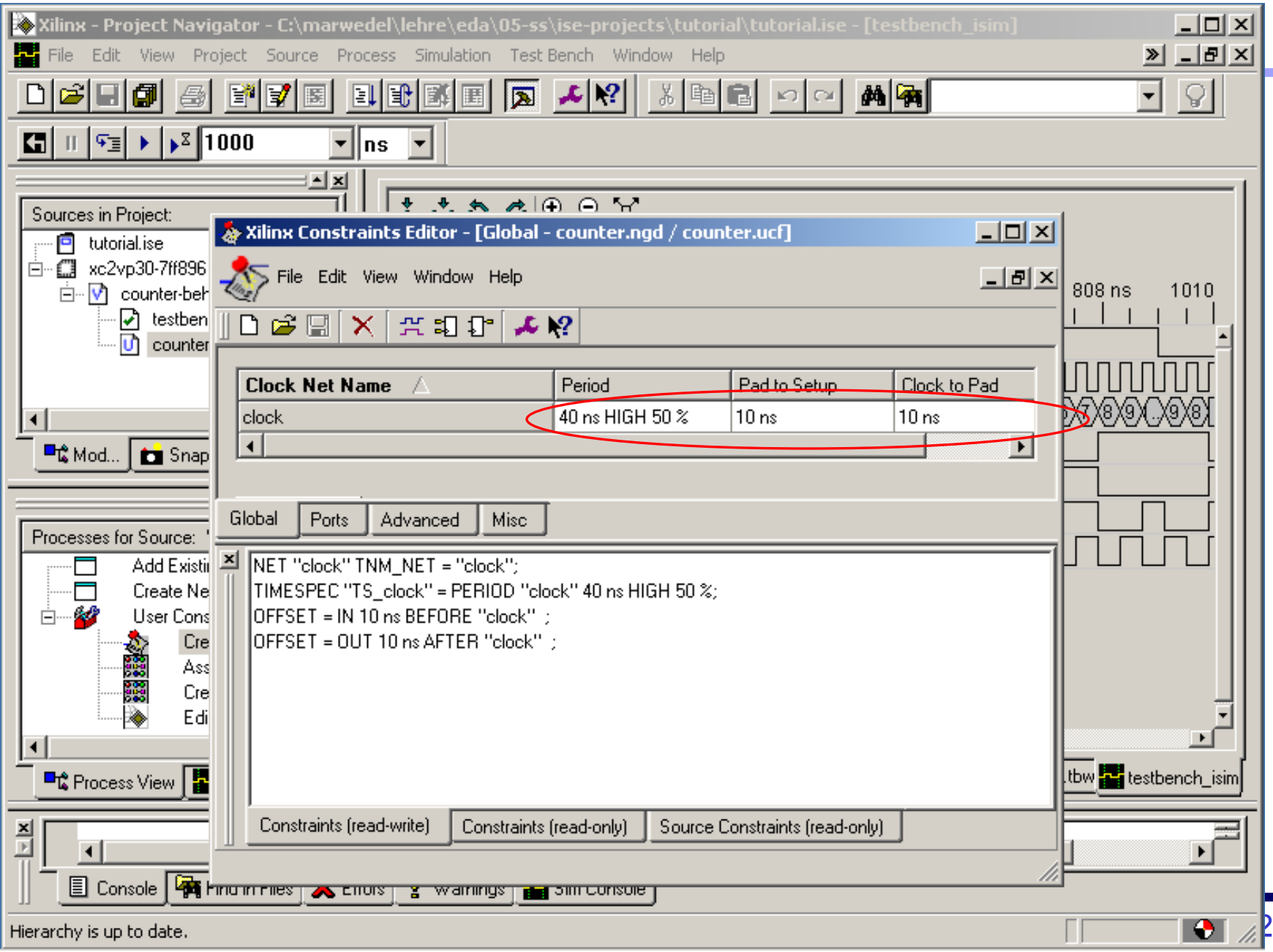


Double click on timing con-straints

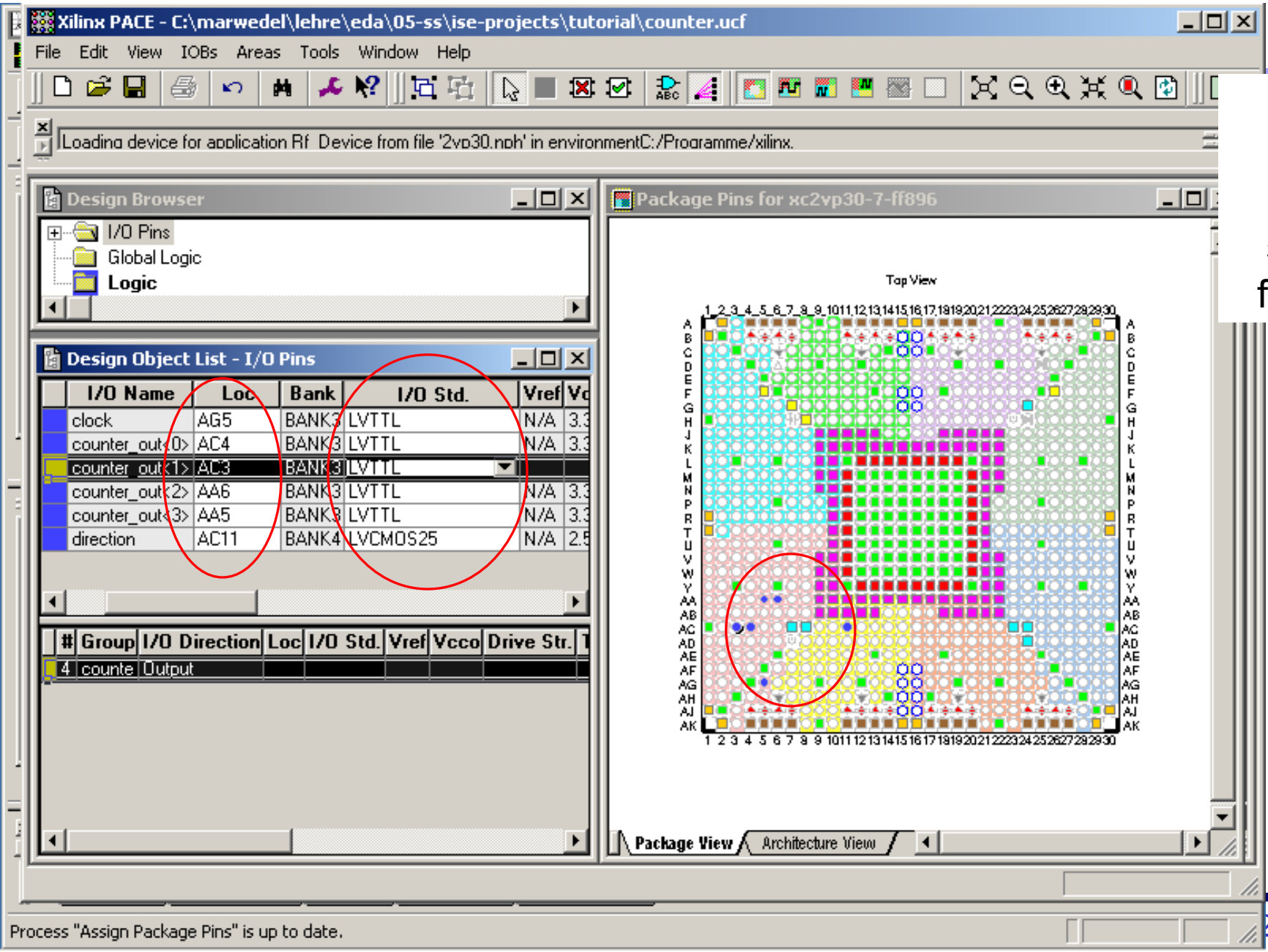
Adding timing constraints (2)



Adding timing constraints (3)

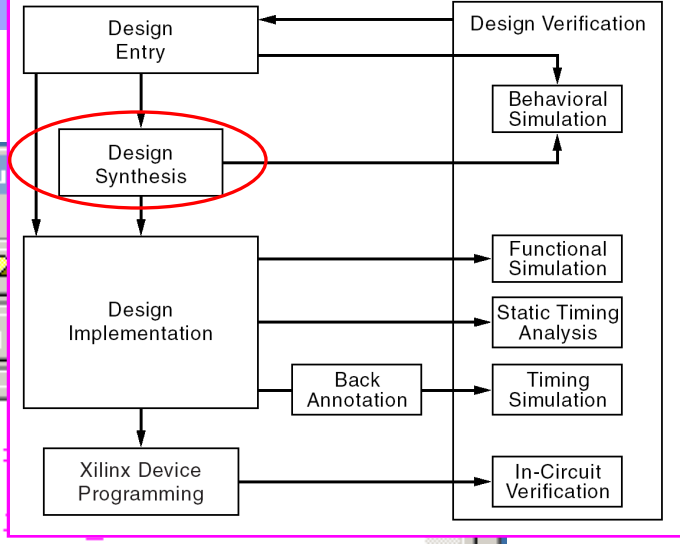


Add pin constraints



Use table from slides fga-01

Synthesis



Xilinx - Project Navigator - C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\tutorial.ise - [cou

File Edit View Project Source Process Simulation Window Help

1000 ns

Sources in Project:
- tutorial.ise
- xc2vp30-7ff896
  - counter-behavioral (counter.vhd)
    - testbench (testbench.tbw)
    - counter.ucf

Modul... Snaps... Library...

Processes for Source: "counter-behavi...
- Create Area Constraint
- Edit Constraints (Text)
- Synthesize - XST
  - View Synthesis Report
  - View RTL Schematic
  - View Technology Sch
  - Check Syntax
  - Generate Post-Synthe
    - Post-Synthesis
- Implement Design
  - Translate

Process View Hierarchy - test...

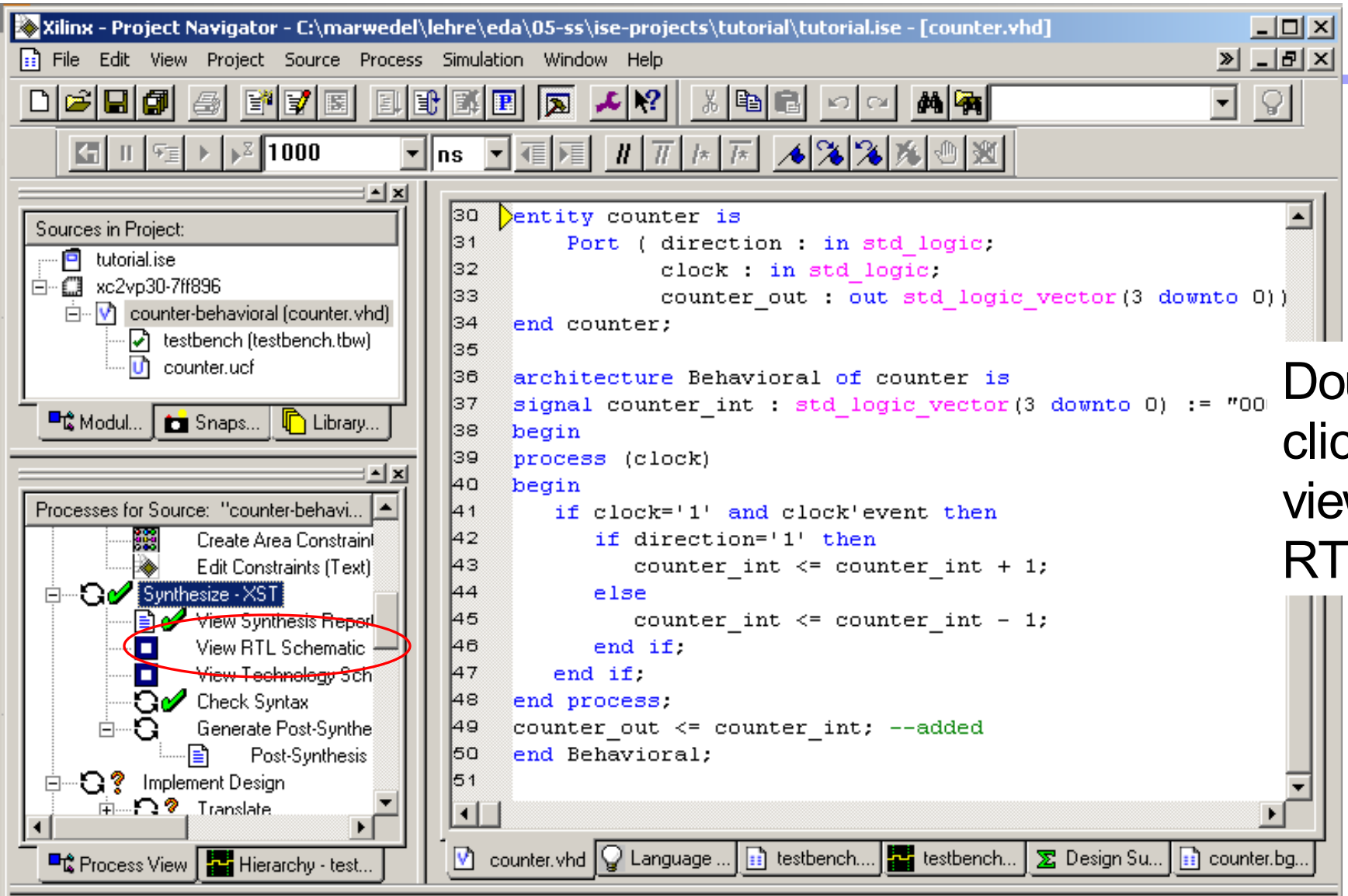
```
30  entity counter is
31      Port ( direction : in std_logi
32             clock : in std_logic;
33             counter_out : out std_
34  end counter;
35
36  architecture Behavioral of counter is
37  signal counter_int : std_logic_vector(3 downto 0) := "0000
38  begin
39  process (clock)
40  begin
41     if clock='1' and clock'event then
42        if direction='1' then
43           counter_int <= counter_int + 1;
44        else
45           counter_int <= counter_int - 1;
46        end if;
47     end if;
48  end process;
49  counter_out <= counter_int; --added
50  end Behavioral;
51
```

counter.vhd Language ... testbench.... testbench... Design Su... counter.bg...

Console Find in Files Errors Warnings

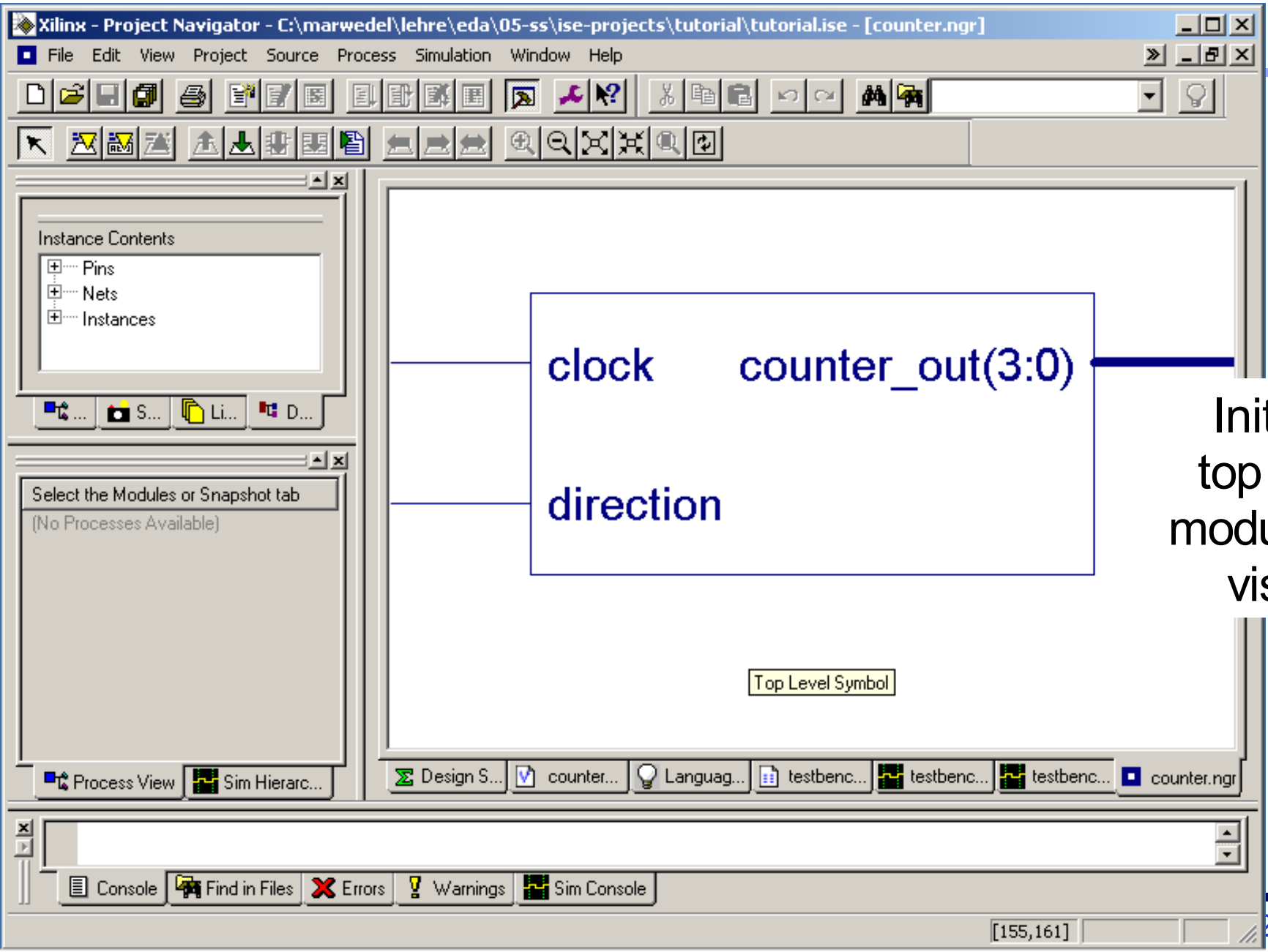
Hierarchy is up to date. Ln 47 Col 12 VHDL

Viewing synthesis results (1)



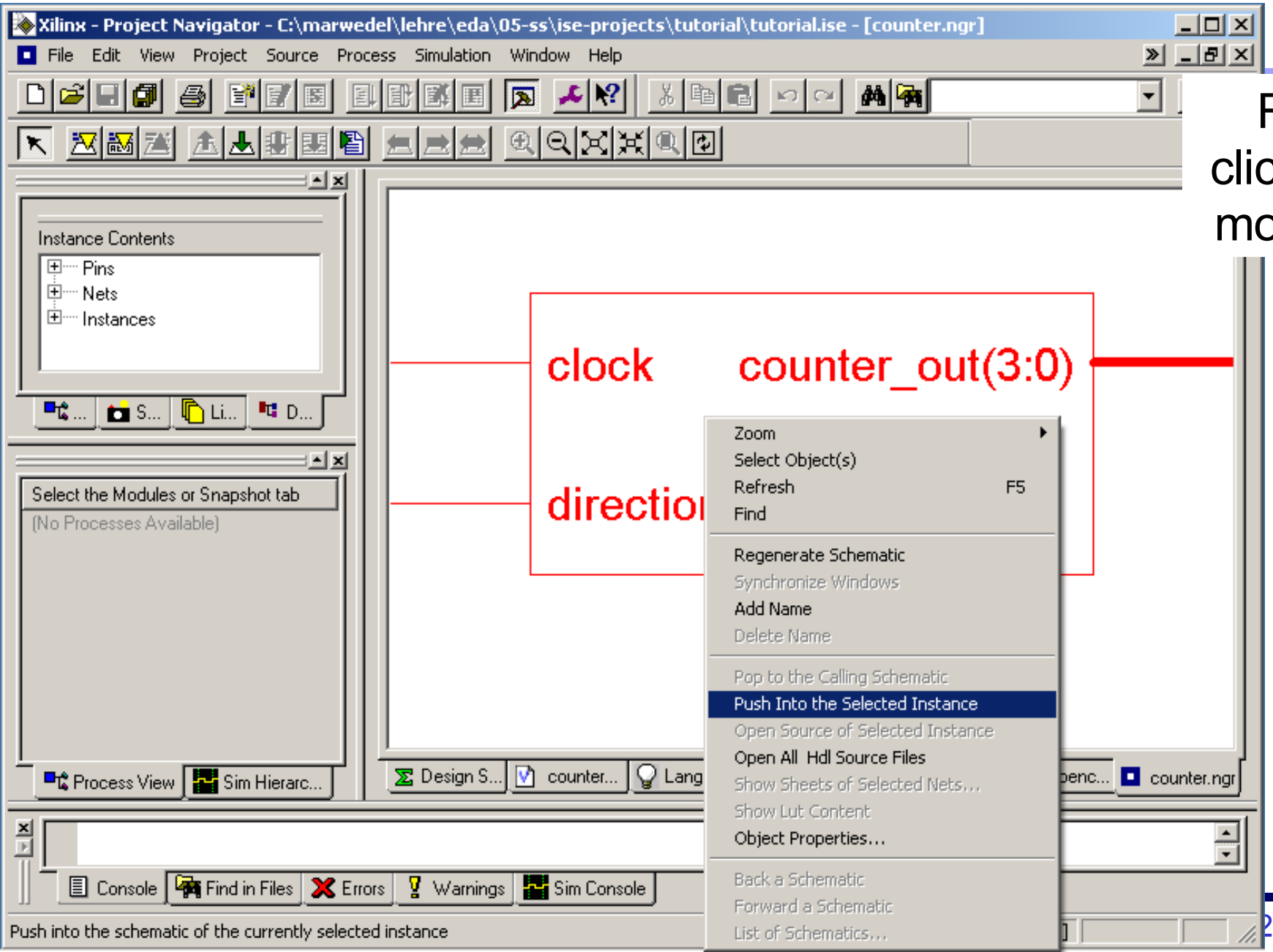
Double click on view RTL

Viewing synthesis results (2)



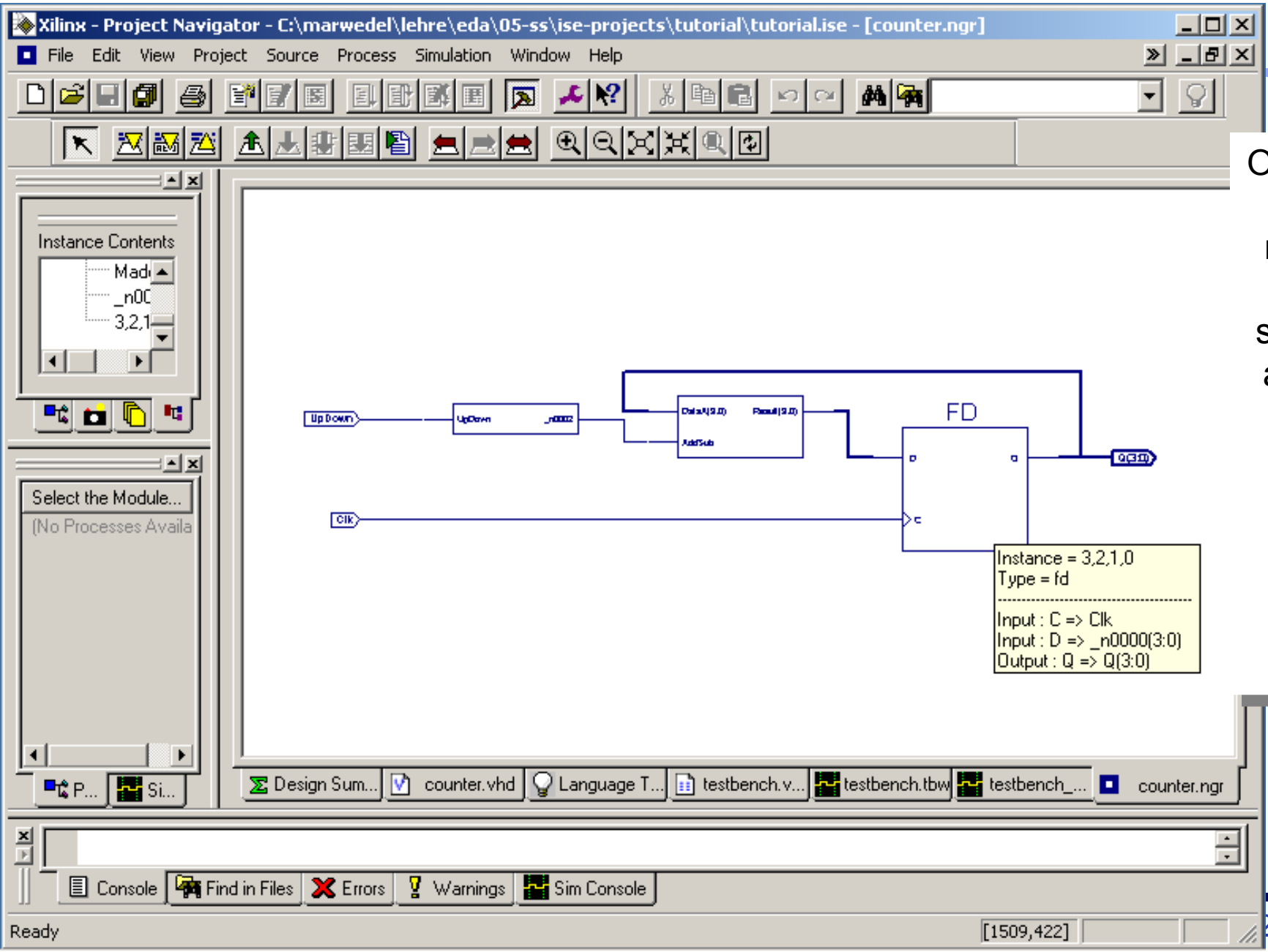
Initially, top level module is visible.

Enter lower level of the hierarchy (1)



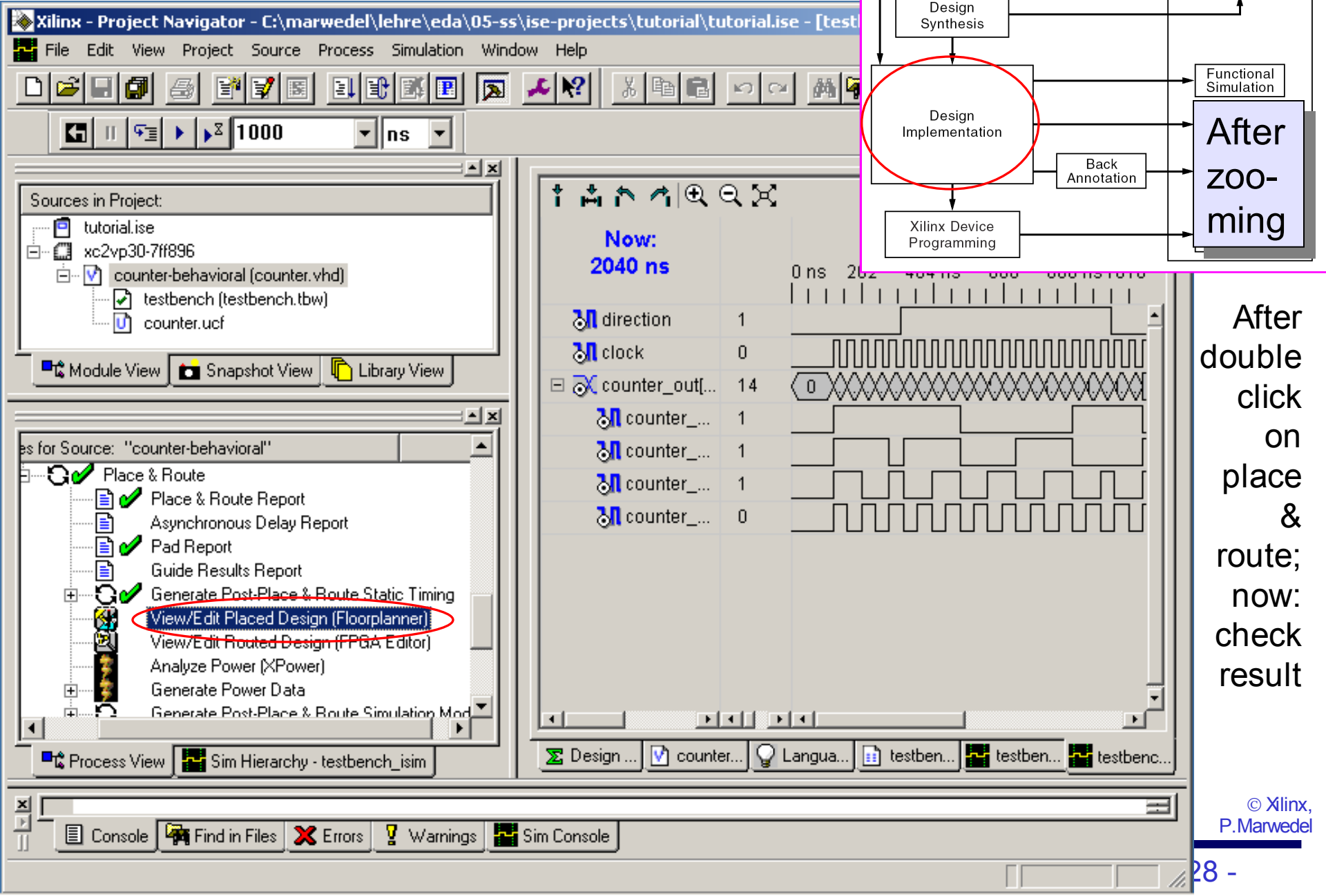
Right click on module

Enter lower level of the hierarchy (2)



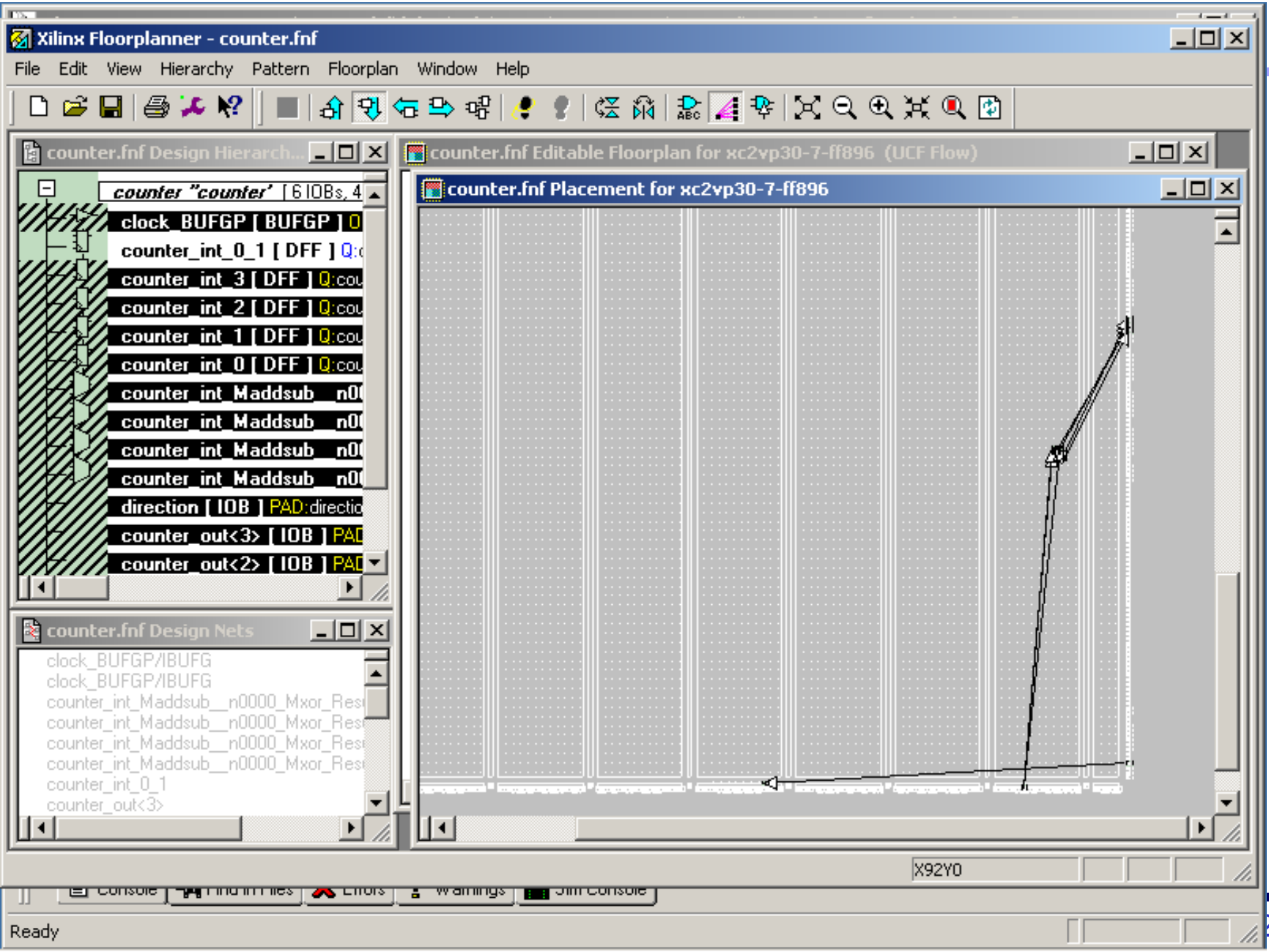
Oops: no counter register, but separate add/sub component; Additional buffers generated

After placement & routing



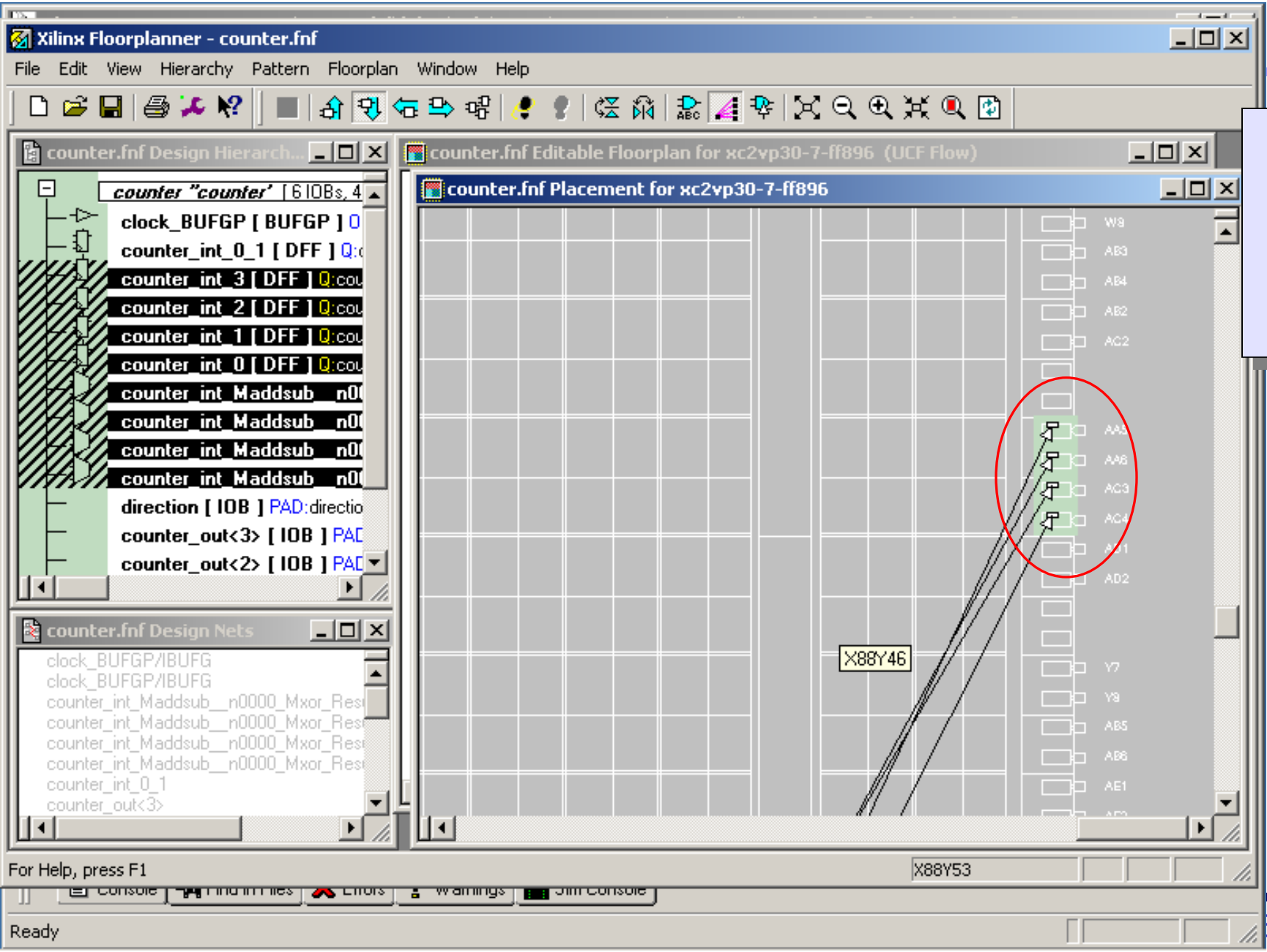
After double click on place & route; now: check result

View result of placement and routing (1)



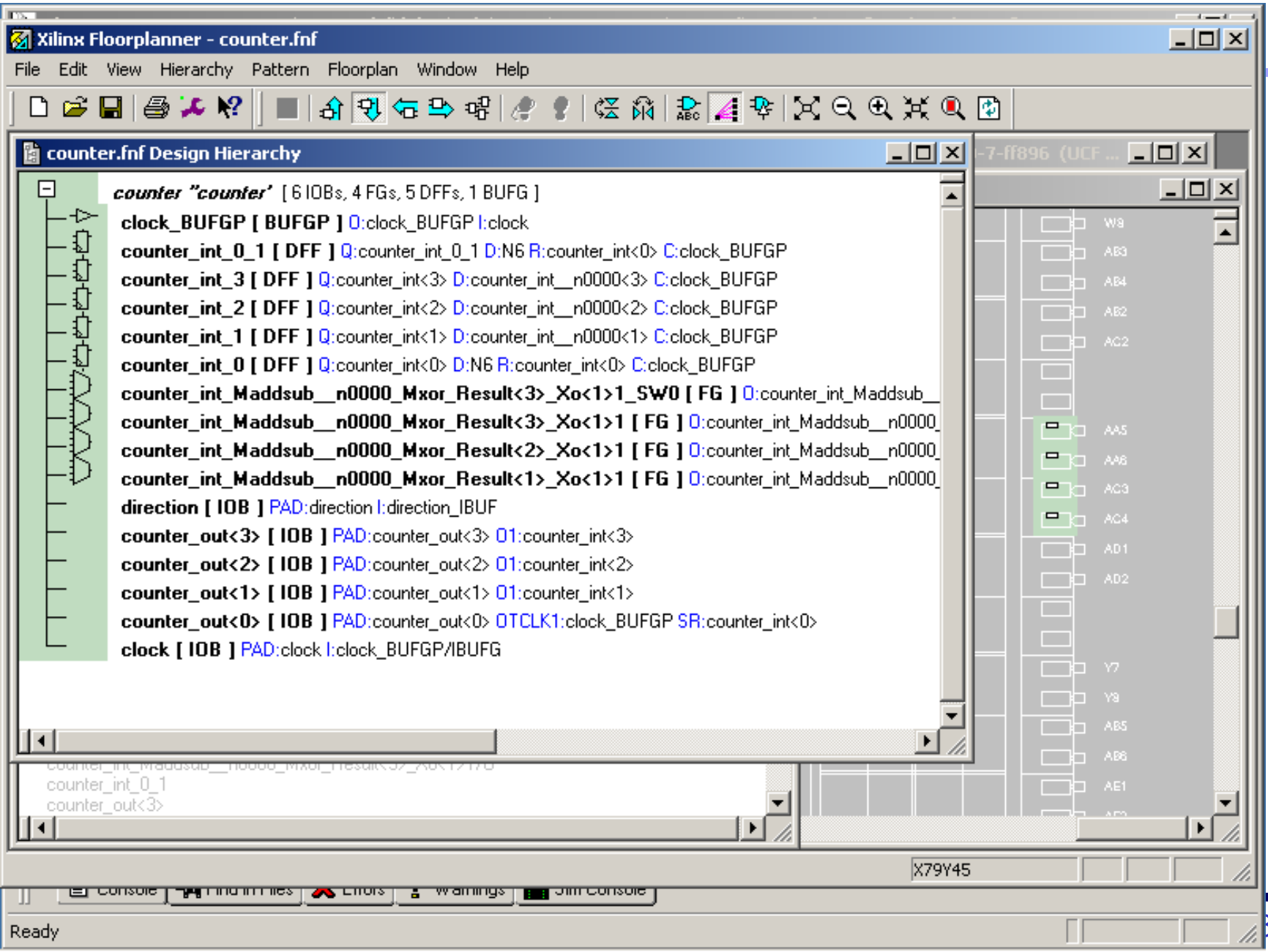
After zoo-ming

View result of placement and routing (2)



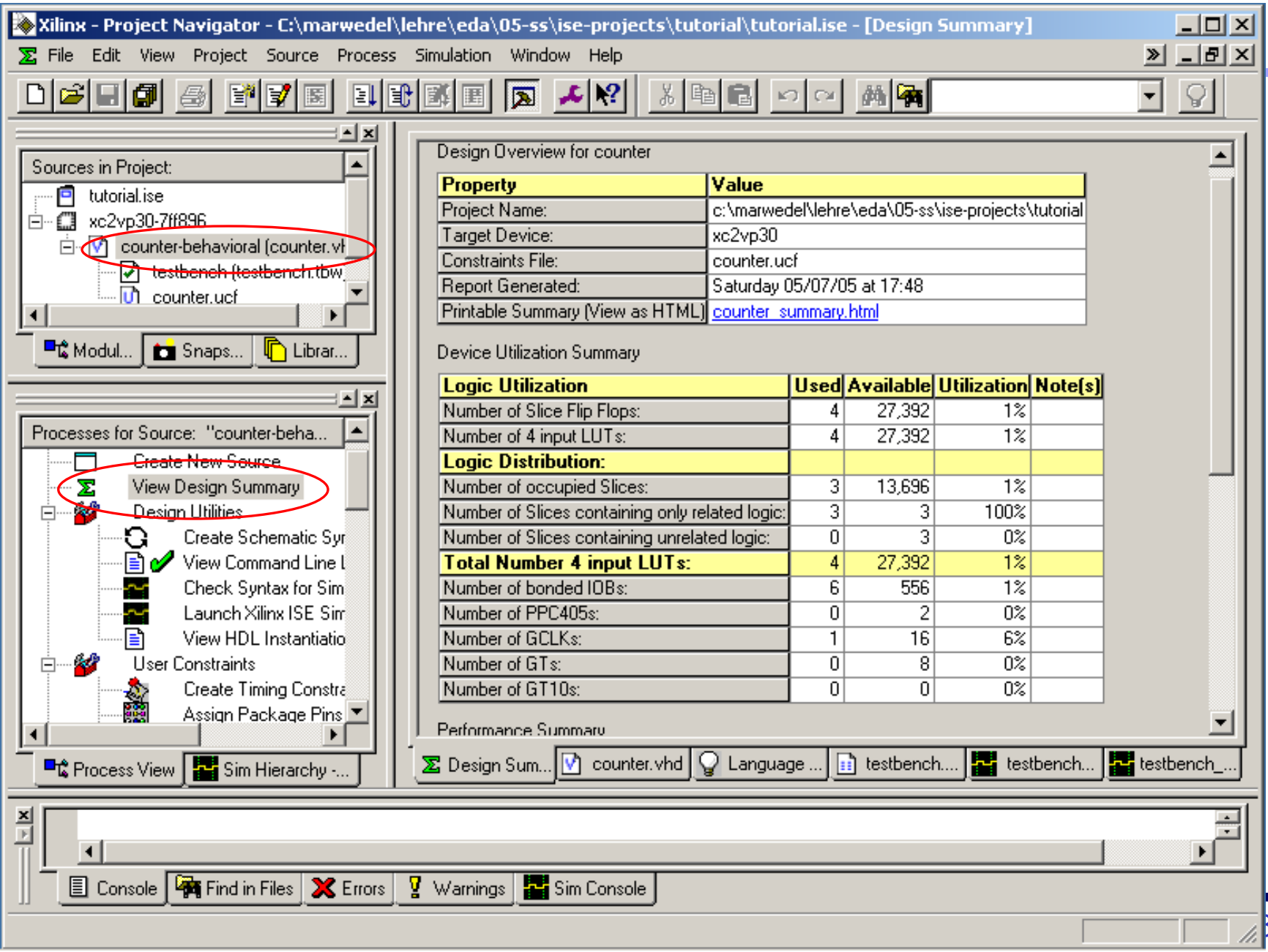
After zoo-ming even more

List of used components

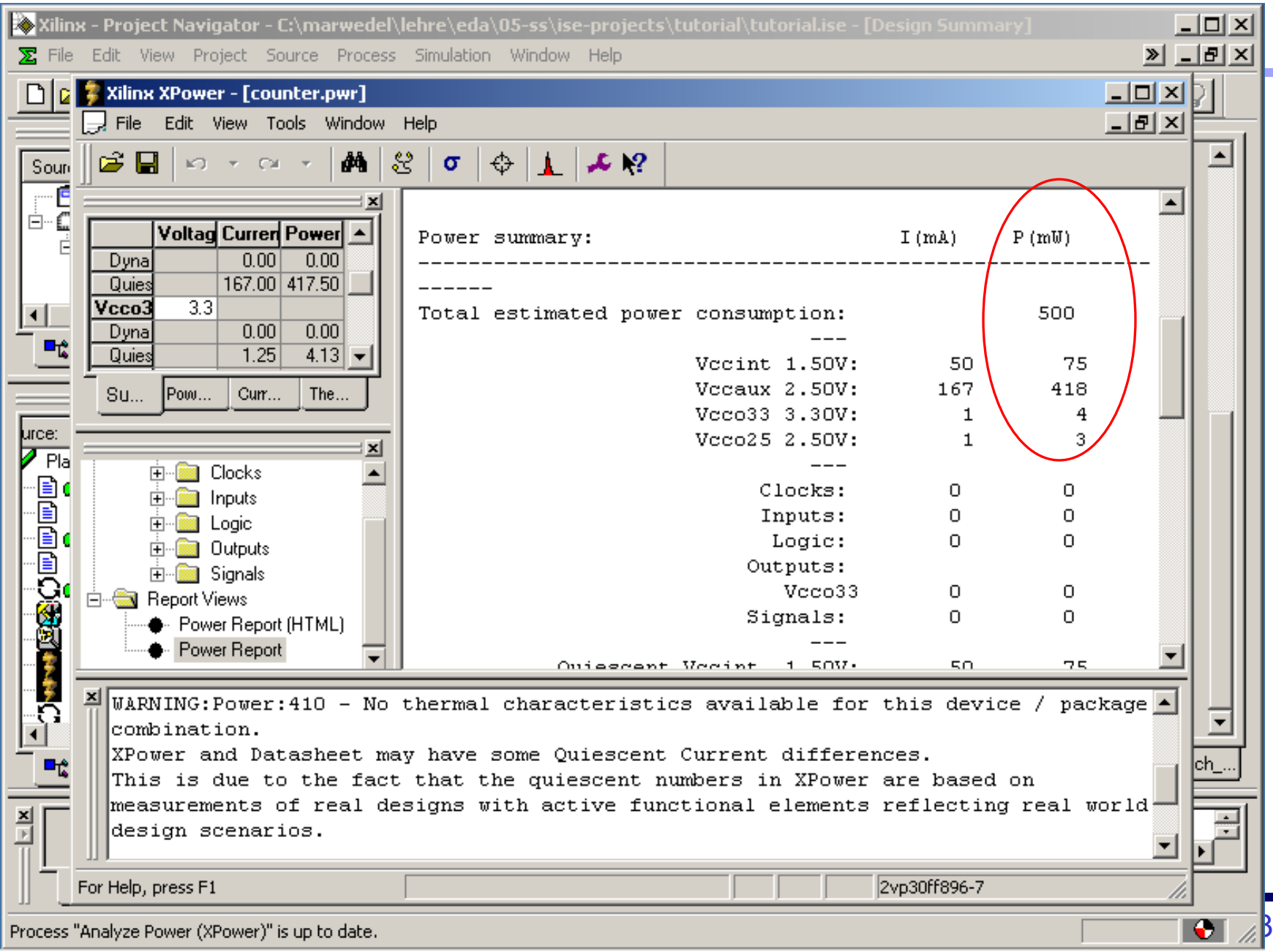


After enlarging left window

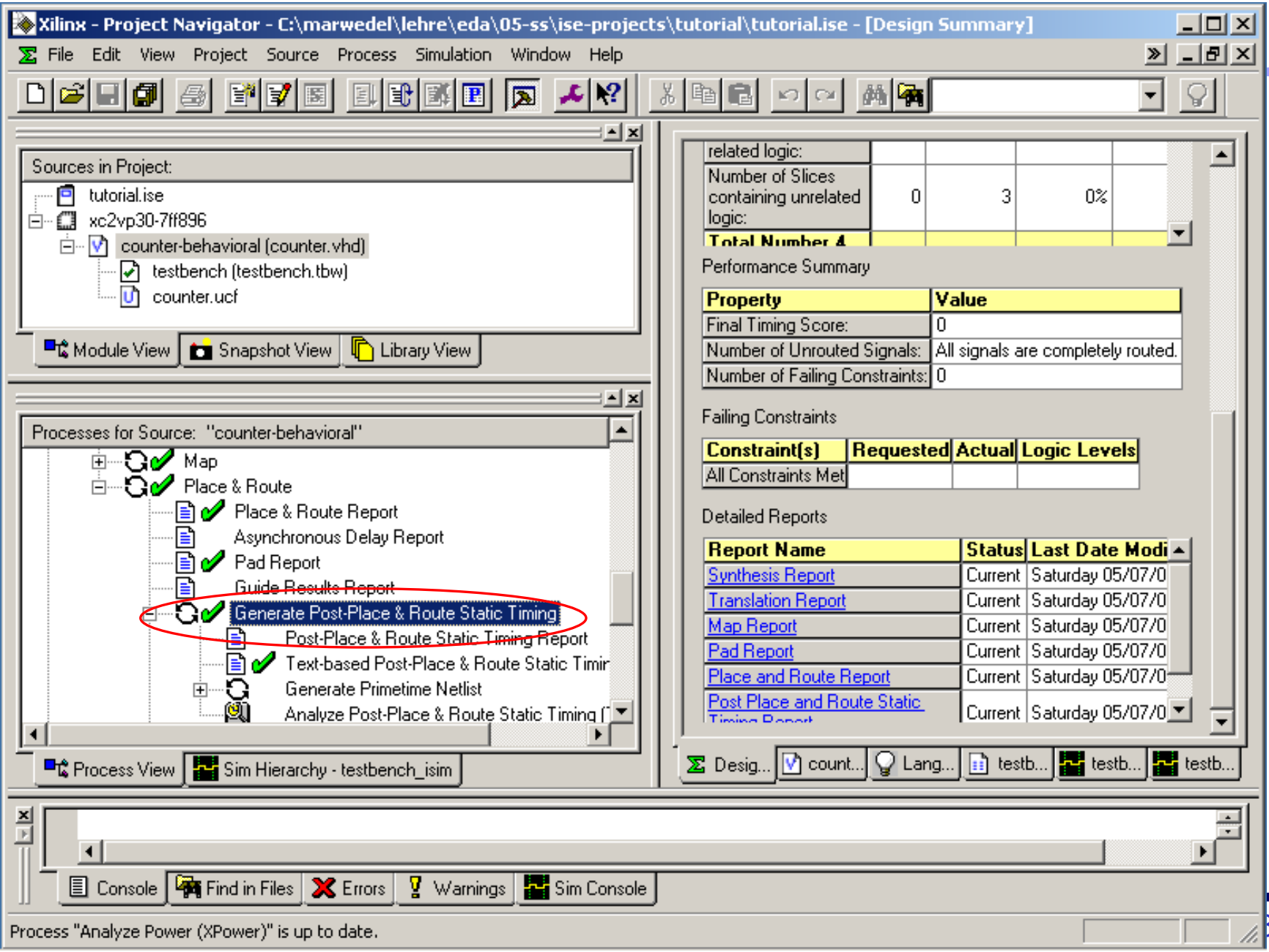
Viewing the design summary



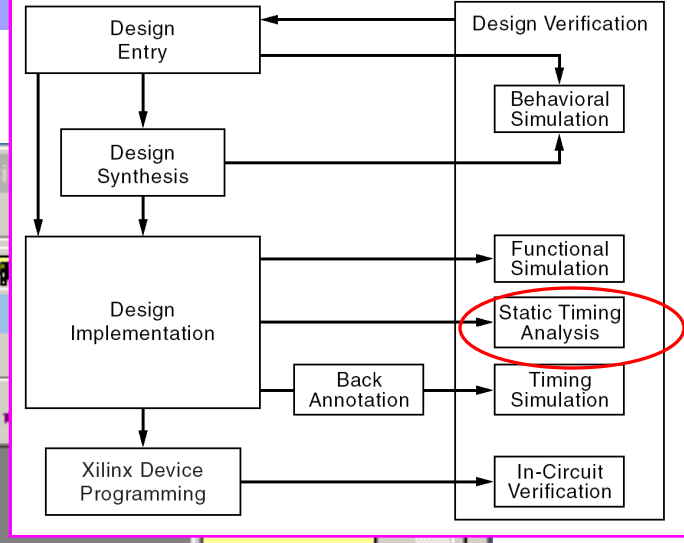
Estimated power consumption



Generate Post-Place & Route Static Timing



Checking Timing constraints (1)



Xilinx - Project Navigator - C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\tutorial.ise - [Desi

File Edit View Project Source Process Simulation Window Help

Xilinx Timing Analyzer - counter.ncd

File Edit View Analyze Window Help

Against Timing Constraints...
Against Auto Generated Design Constraints...
Against User Specified Paths
Constraints Interaction...
Query Nets...
Query Timegroups...
Reset All Path Filters

```
1 >OpenDesign NoDefaultPCF C:\marwedel\lehre\eda\05-ss\ise-projects\
Loading device for application Rf_Device from file '2vp30.nph' in en
   "counter" is an NCD, version 3.1, device xc2vp30, package ff896,
2 >OpenPCF C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\counter
```

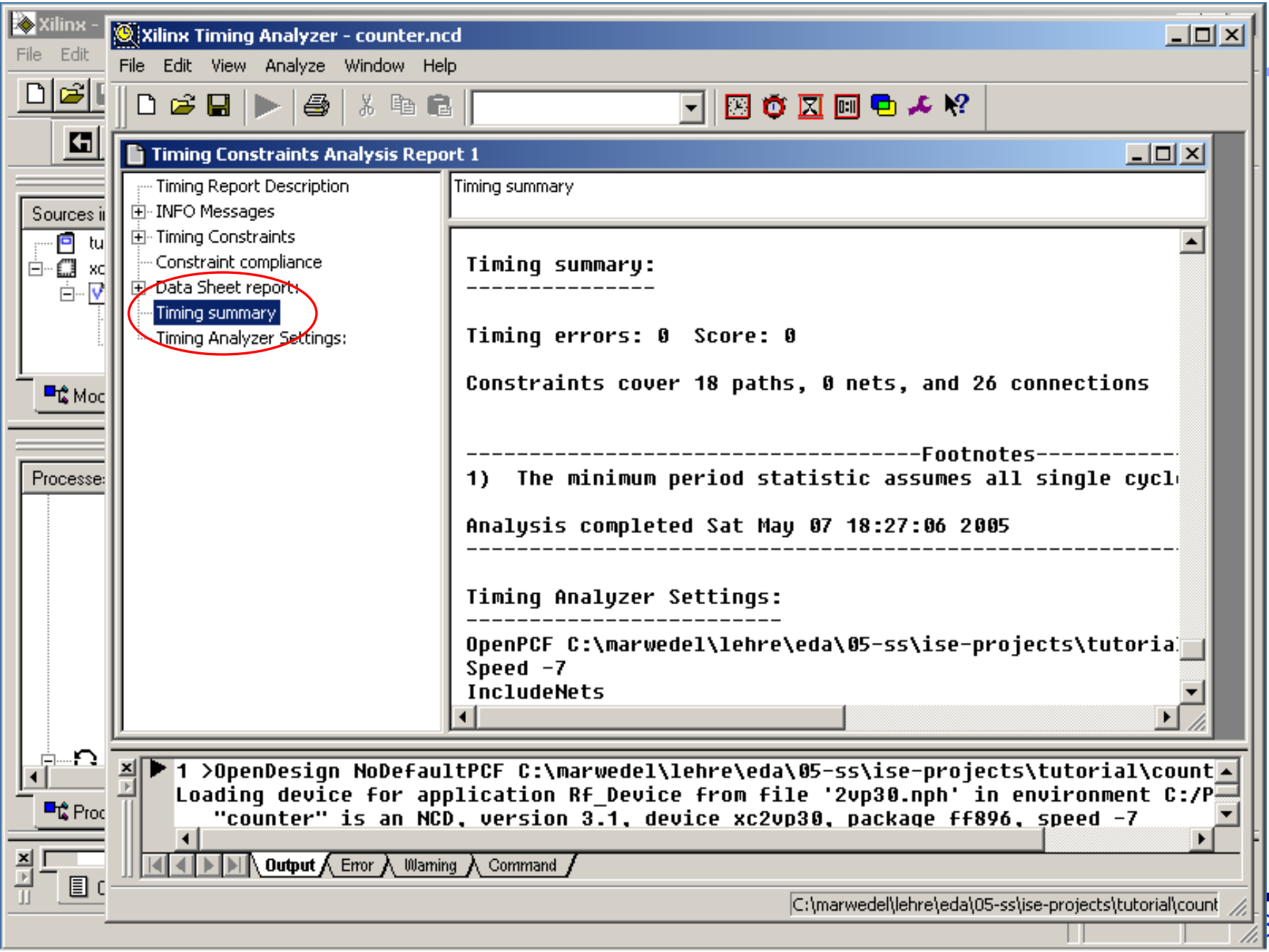
Output Error Warning Command

Perform a timing constraints analysis, reporting on all paths covered by timi C:\marwedel\lehre\eda\05-ss\ise-projects\

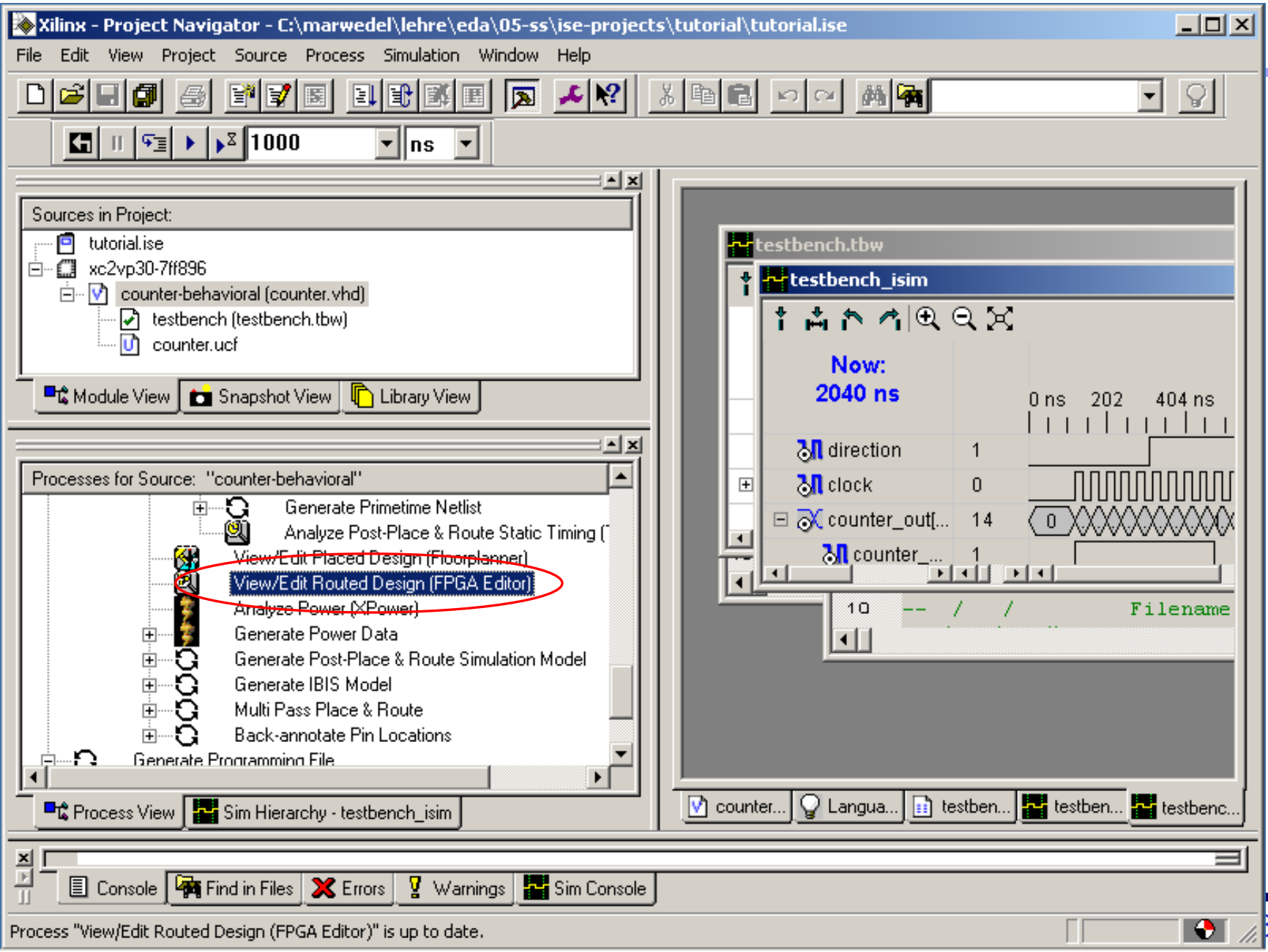
Console Find in Files Errors Warnings Sim Console

Process "Analyze Post-Place & Route Static Timing (Timing Analyzer)" is up to date.

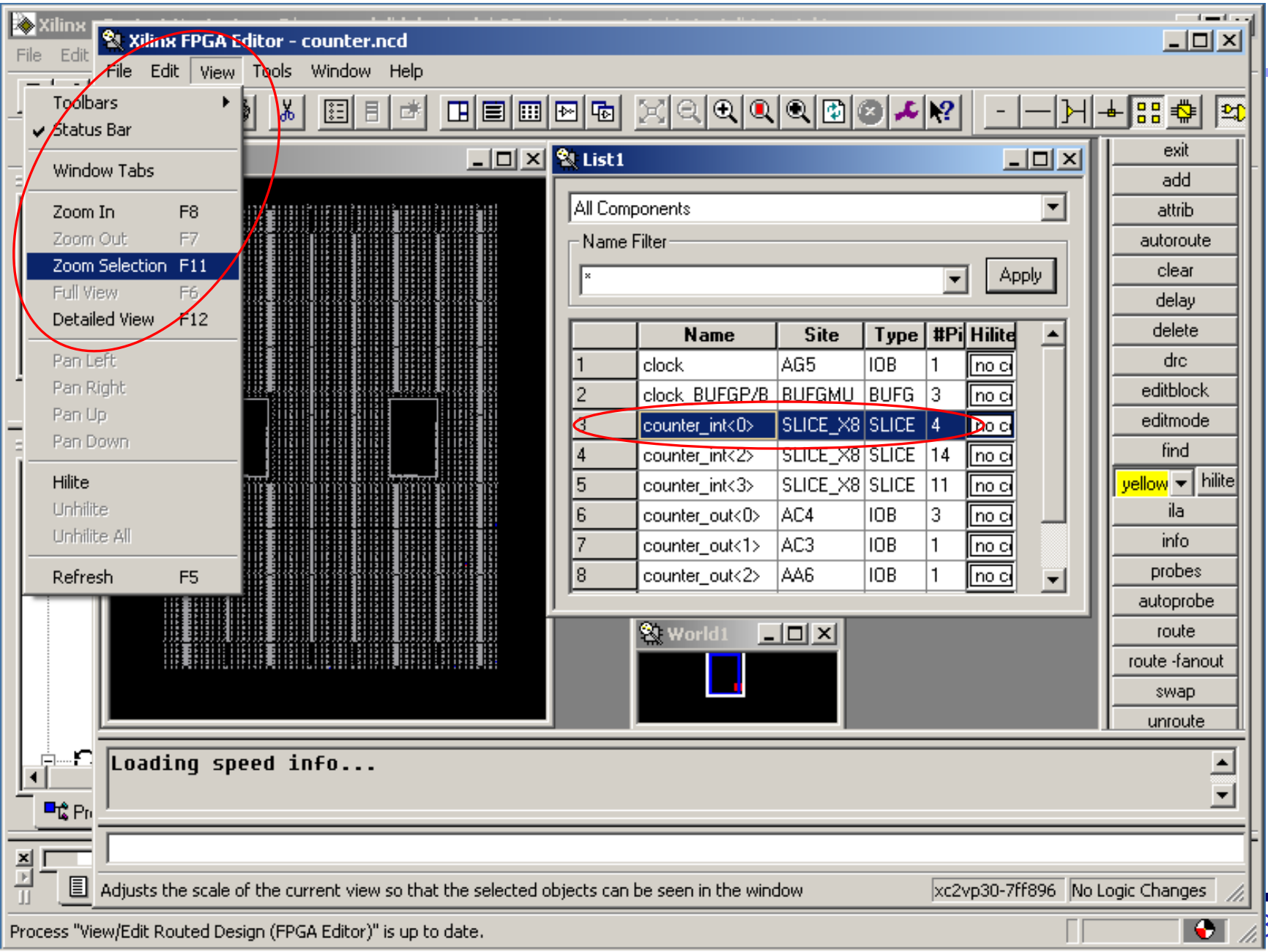
Checking Timing constraints (2)



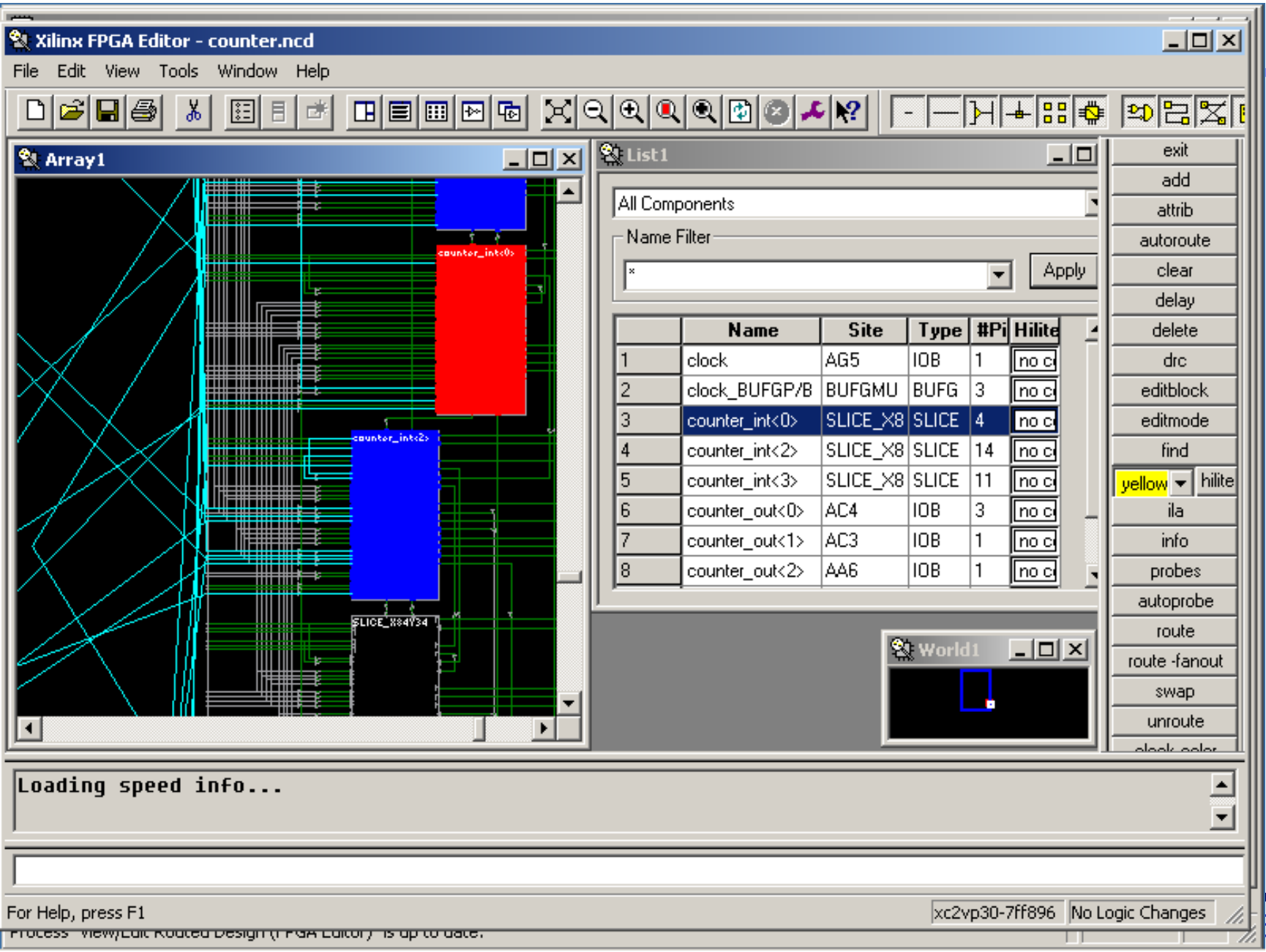
View routed design (1)



View routed design (2)

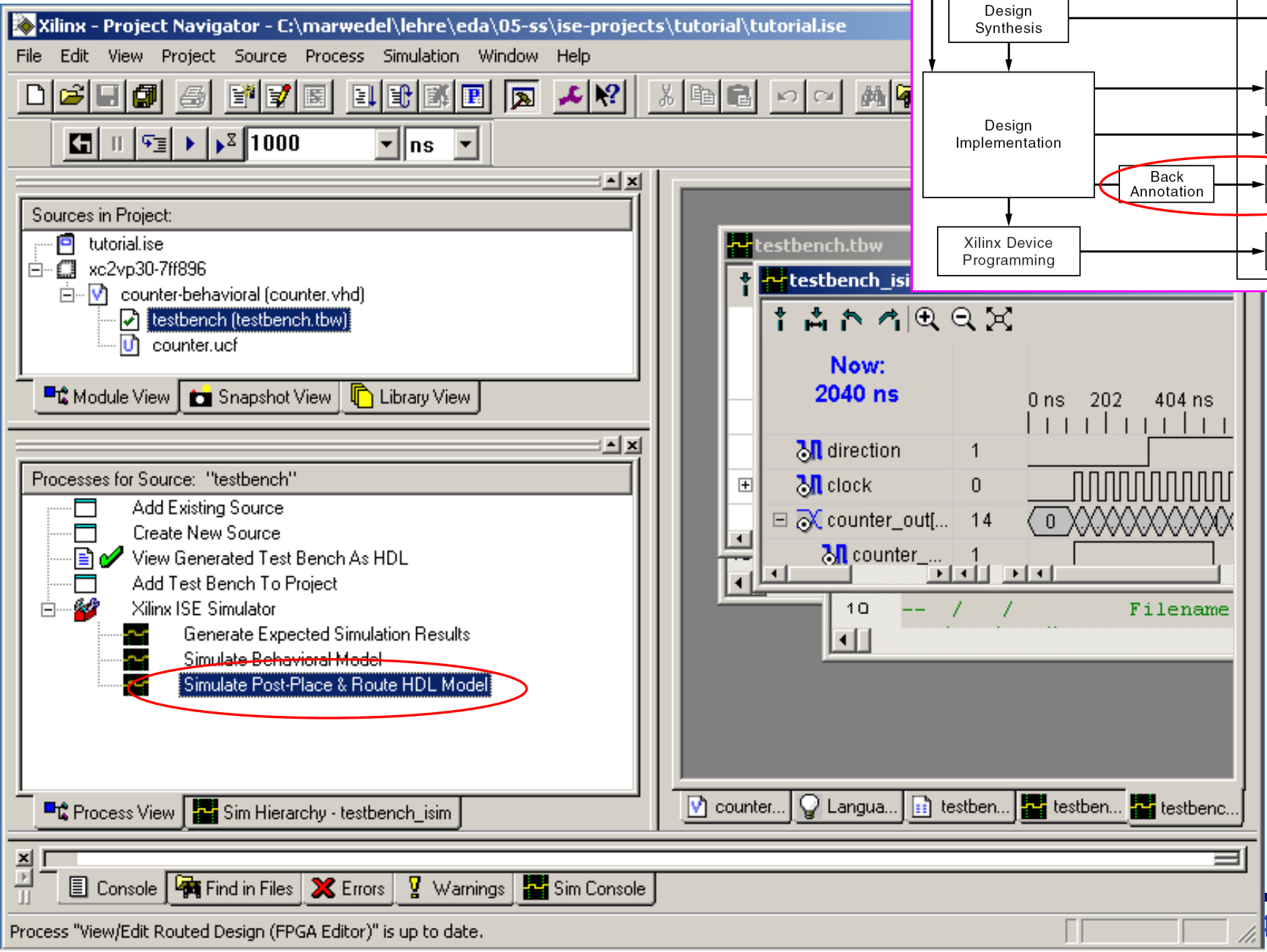


View routed design (3)

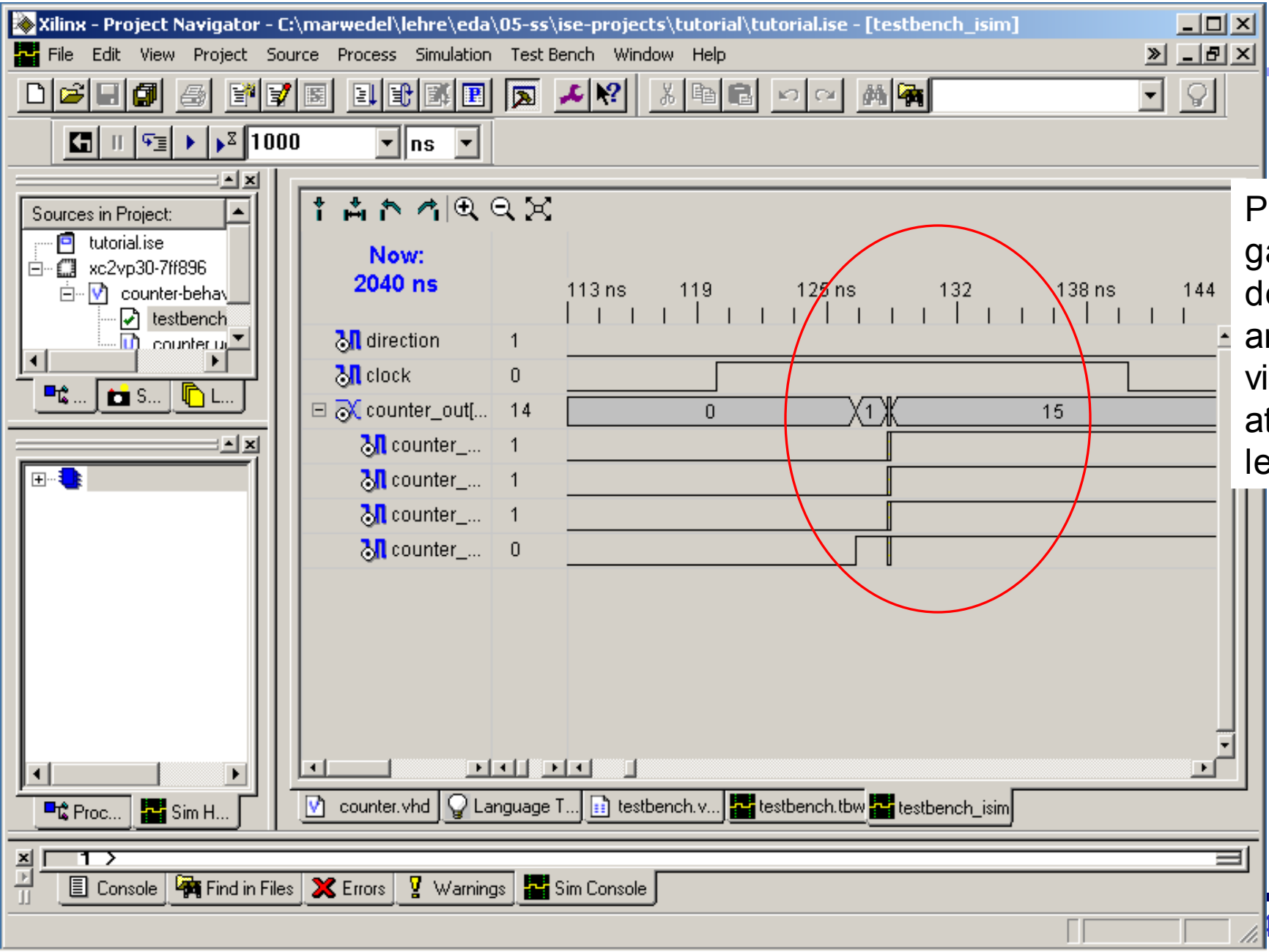


4 slices in 1 CLB used

Simulate Post-Place & Route HDL Model (1)

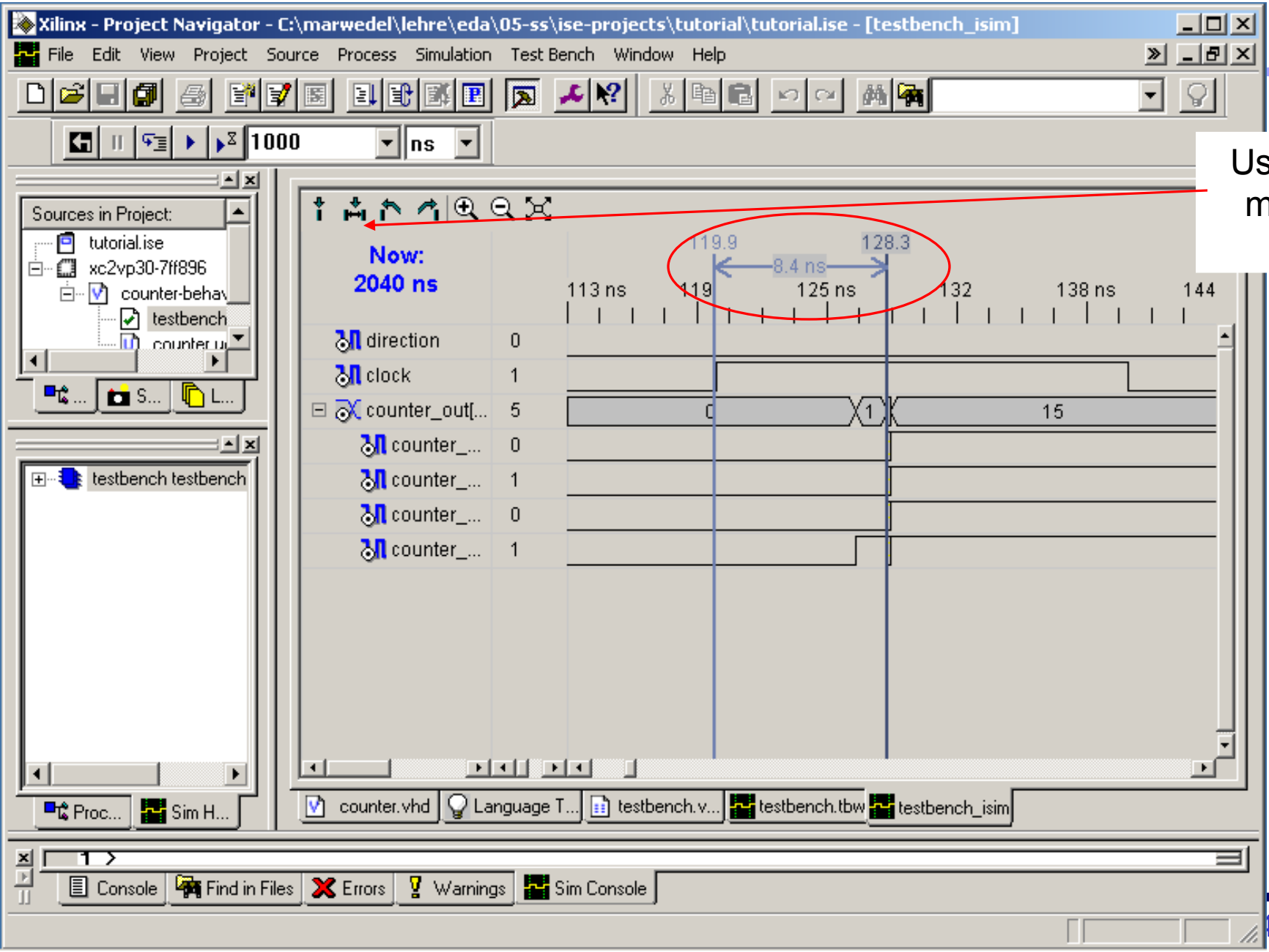


Simulate Post-Place & Route HDL Model (2)



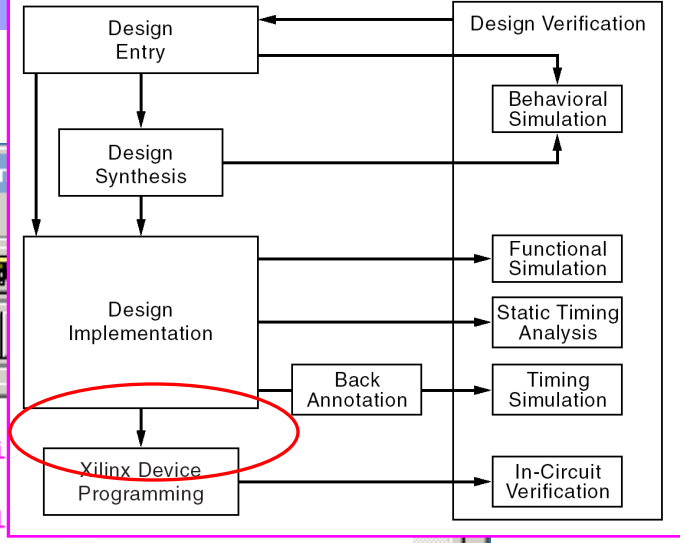
Propa-gation delays are visible at this level

Simulate Post-Place & Route HDL Model (3)



Using the measure marker

Generation of configuration file



Xilinx - Project Navigator - C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\tutorial.ise - [cour

File Edit View Project Source Process Simulation Window Help

1000 ns

Sources in Project:
- tutorial.ise
- xc2vp30-7ff896
- counter-behavioral (counter.vh
- testbench (testbench.tbw)
- counter.ucf

Modul... Snaps... Library...

Processes for Source: "counter-behavi...
- Analyze Power
- Generate Powe
- Generate Post-I
- Generate IBIS I
- Multi Pass Plac
- Back-annotate
- Generate Programming File
- Programming File Gen
- Generate PROM, ACE
- Configure Device (iMF

Process View Hierarchy - test...

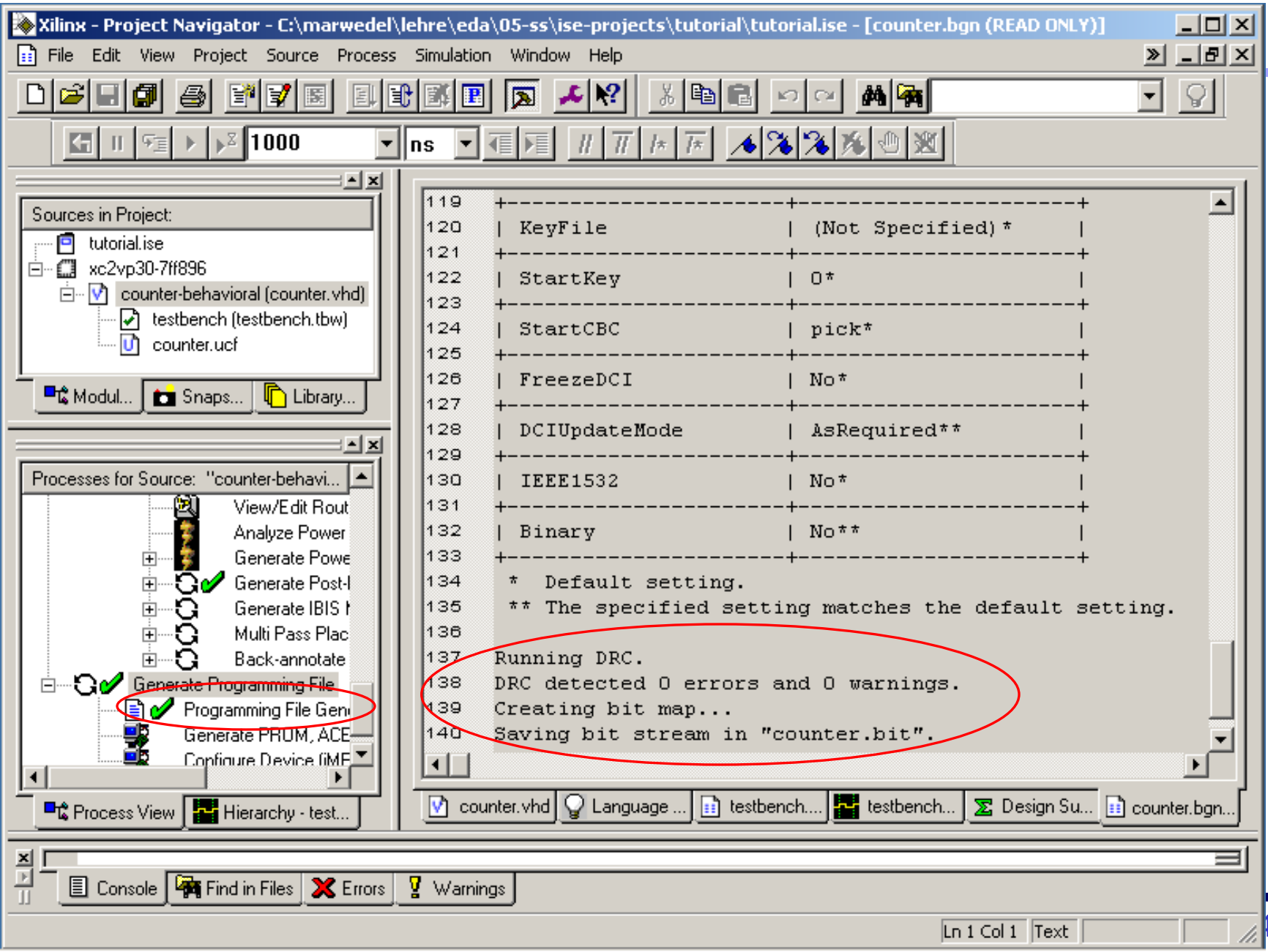
```
30  entity counter is
31      Port ( direction : in std_logi
32             clock : in std_logic;
33             counter_out : out std_l
34  end counter;
35
36  architecture Behavioral of counter is
37  signal counter_int : std_logic_vector(3 downto 0) := "0000
38  begin
39  process (clock)
40  begin
41     if clock='1' and clock'event then
42        if direction='1' then
43           counter_int <= counter_int + 1;
44        else
45           counter_int <= counter_int - 1;
46        end if;
47     end if;
48  end process;
49  counter_out <= counter_int; --added
50  end Behavioral;
51
```

counter.vhd Language T... testbench.v... testbench.tbw

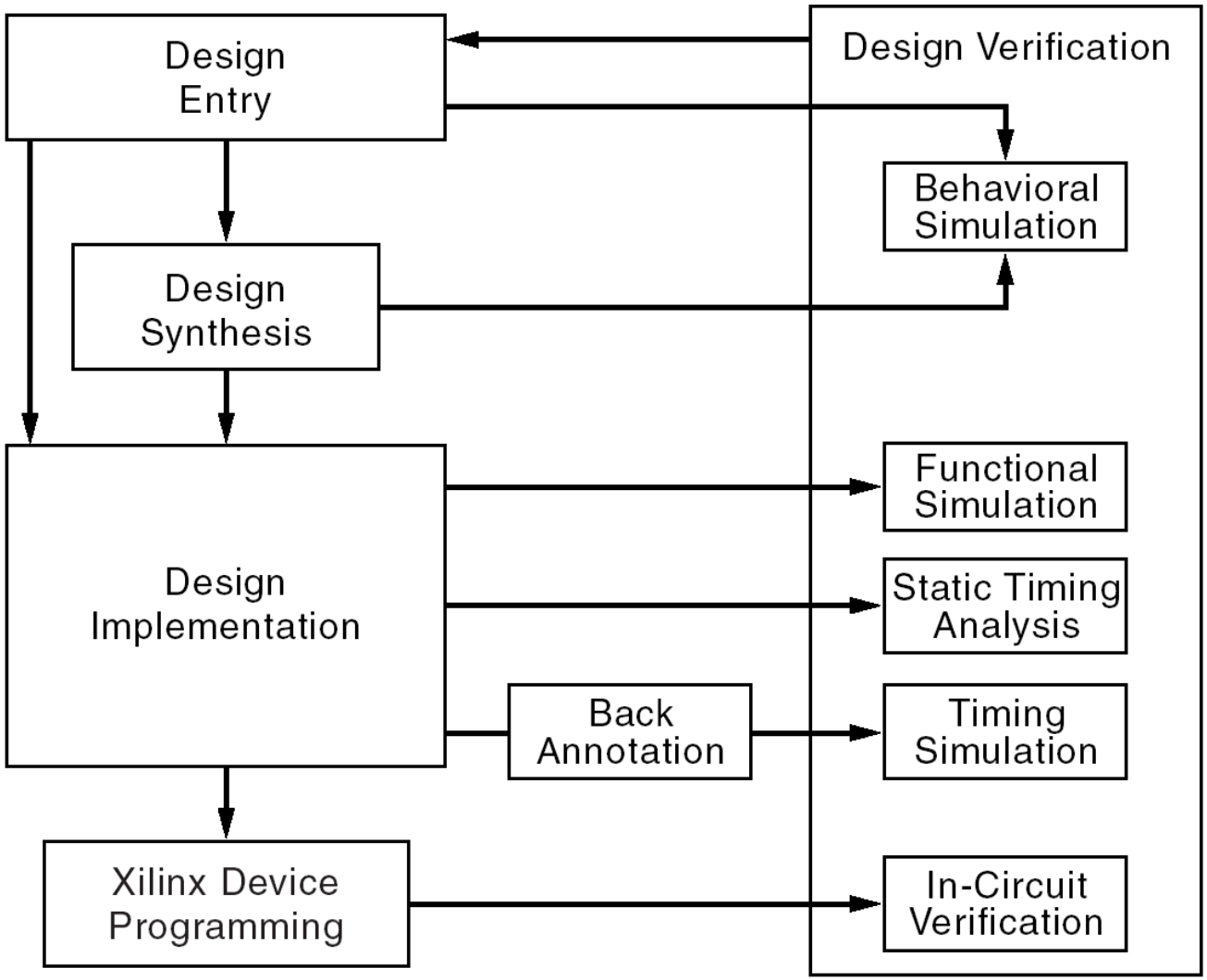
Console Find in Files Errors Warnings

Ln 30 Col 2 VHDL

Generation of configuration file



Summary



Fast path through design flow with Xilinx ISE