



FPGA Synthesis

Example: Counter

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Gliederung

Zeitplan

- Einführung
- SystemC
 - Vorlesungen und Programmierung

3,5 Wochen

- 
- FPGAs
 - Vorlesungen
 - VHDL-basierte Konfiguration von FPGAs mit dem XUP VII Pro Entwicklungssystem

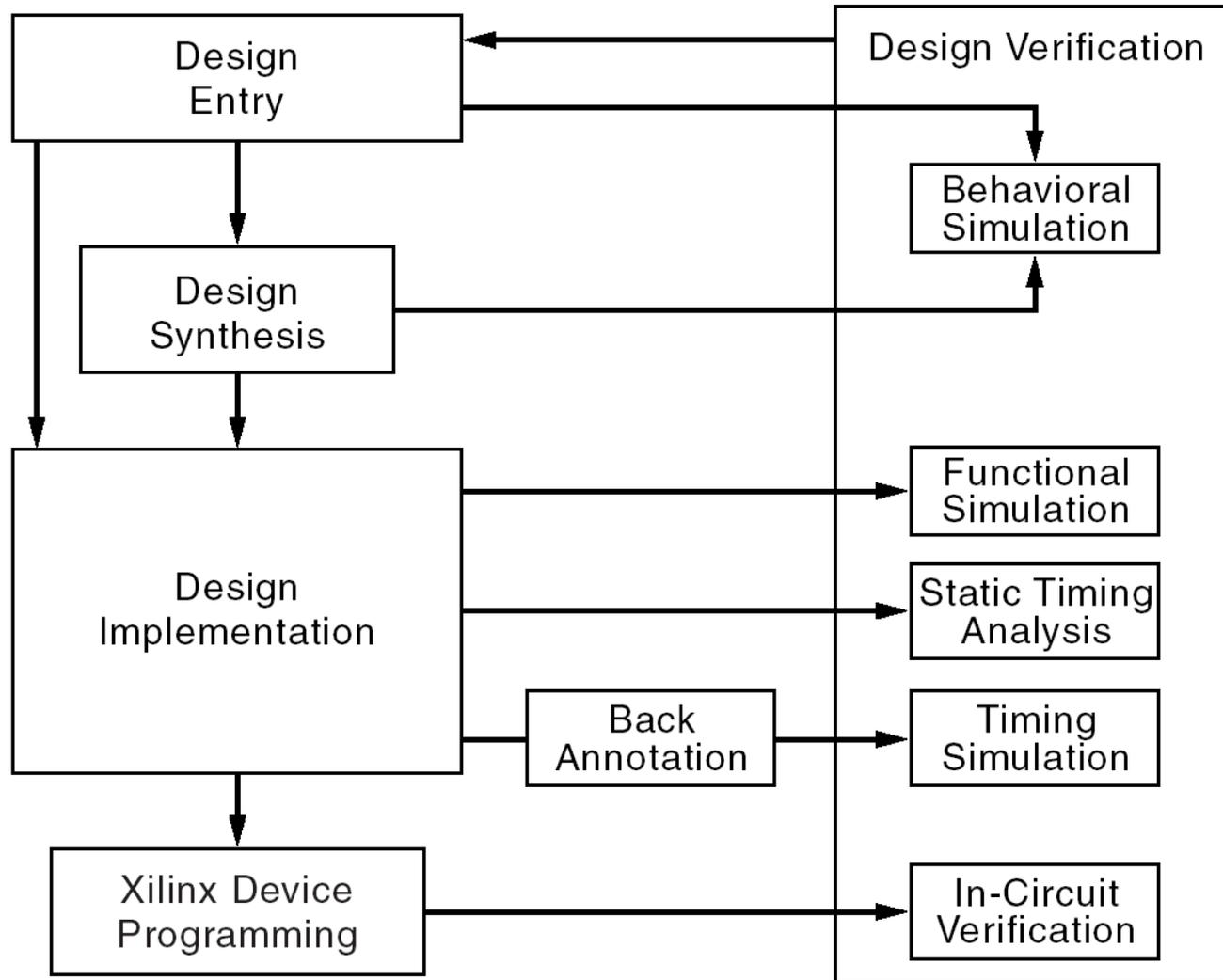
3,5 Wochen

- Algorithmen
 - Mikroarchitektur-Synthese
 - Automaten-synthese
 - Logik-synthese
 - Layout-synthese

6 Wochen

ISE design flow

http://www.xilinx.com/support/sw_manuals/xilinx8/download/qst.zip



Starting a more complex design example

New Project

Enter a Name and Location for the Project

Project Name: Project Location: ...

Select the type of Top-Level module for the Project

Top-Level Module Type:

< Zurück Weiter > Abbrechen Hilfe

Set simulator to ISE for installations without separate Modelsim simulator.

Sources in Project:
(No Project Open)

Processes for Source:
(No Processes Available)

(Empty Log)

Console Find in Files Errors Warnings

Hierarchy is up to date.

Some slides use patched project name

Generated design header

The screenshot displays the Xilinx Project Navigator IDE. The main window shows the source code for a VHDL file named 'counter.vhd'. The code defines a counter entity and its behavioral architecture.

Sources in Project:

- tutorial ise
- xc2vp30-7ff896
- counter-behavioral (counter.vhd)

Processes for Source: "counter-behavioral"

- Add Existing Source
- Create New Source
- View Design Summary
- Design Utilities
 - Create Schematic Symb
 - View Command Line Lo
 - View HDL Instantiation
 - User Constraints

Main Code Editor (counter.vhd):

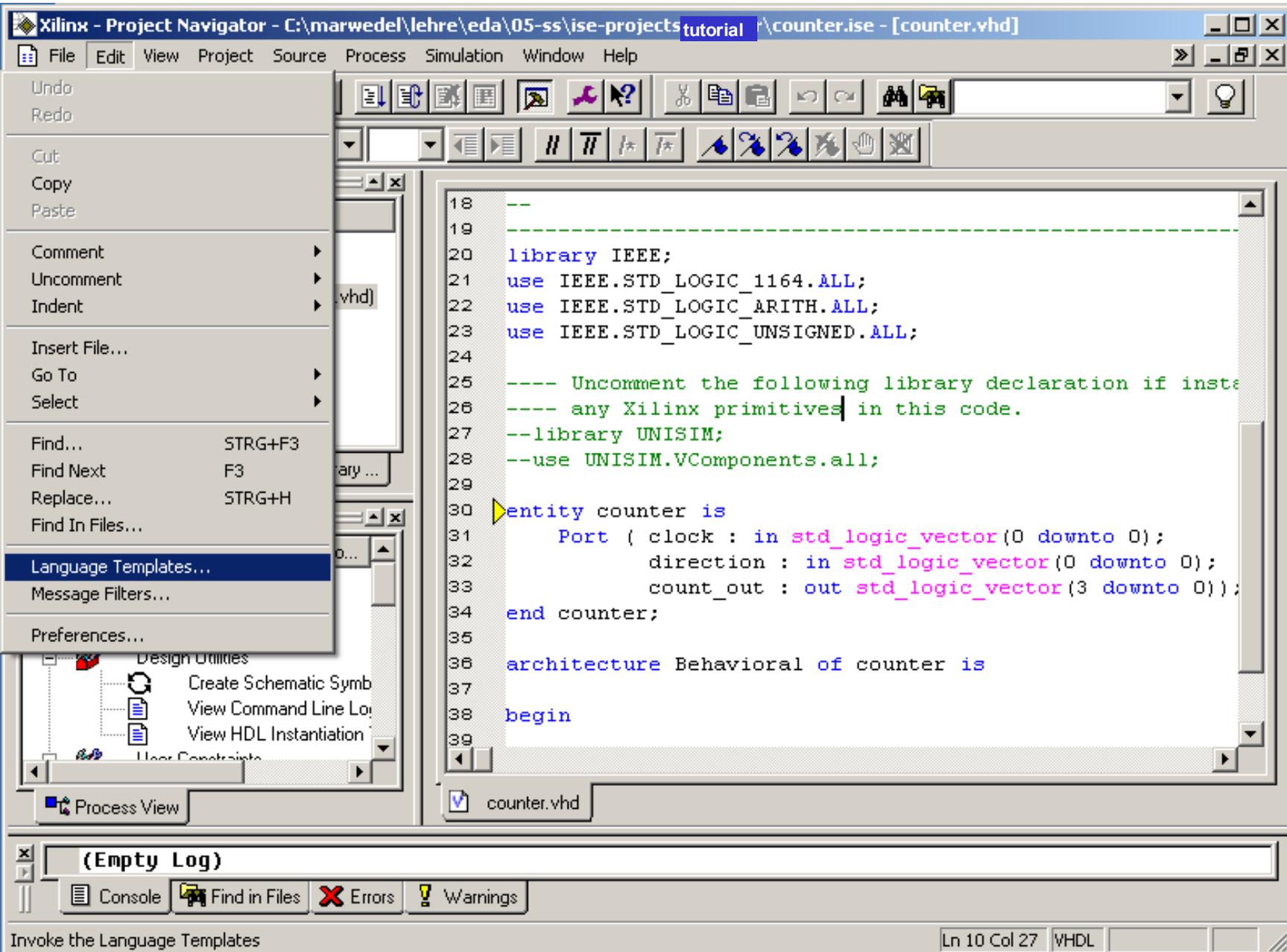
```

20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 use IEEE.STD_LOGIC_ARITH.ALL;
23 use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25 ---- Uncomment the following library declaration if inste
26 ---- any Xilinx primitives in this code.
27 --library UNISIM;
28 --use UNISIM.VComponents.all;
29
30 entity counter is
31     Port ( clock : in std_logic_vector(0 downto 0);
32           direction : in std_logic_vector(0 downto 0);
33           count_out : out std_logic_vector(3 downto 0) );
34 end counter;
35
36 architecture Behavioral of counter is
37
38 begin
39
40
41 end Behavioral;
  
```

Console: (Empty Log)

Ln 1 Col 1 VHDL

Using language templates to define architectural body



The screenshot shows the Xilinx Project Navigator interface. The 'Edit' menu is open, and the 'Language Templates...' option is highlighted. The main editor window displays the following VHDL code:

```
18  --
19  -----
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.STD_LOGIC_ARITH.ALL;
23  use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25  ---- Uncomment the following library declaration if inste
26  ---- any Xilinx primitives in this code.
27  --library UNISIM;
28  --use UNISIM.VComponents.all;
29
30  entity counter is
31      Port ( clock : in std_logic_vector(0 downto 0);
32            direction : in std_logic_vector(0 downto 0);
33            count_out : out std_logic_vector(3 downto 0));
34  end counter;
35
36  architecture Behavioral of counter is
37
38  begin
39
```

The status bar at the bottom indicates 'Ln 10 Col 27 VHDL'.

Open
edit
menu

Select simple counter

The screenshot shows the Xilinx Project Navigator interface. The main window displays a tree view of templates under the 'Counters' folder. The 'Simple Counter' template is selected. The right pane shows the VHDL code for the selected template, which is a simple counter process.

```
process (<clock>)
begin
    if <clock>='1' and <clock>'event
        if <count_direction>='1' then
            <count> <= <count> + 1;
        else
            <count> <= <count> - 1;
        end if;
    end if;
end process;
```

The interface includes a menu bar (File, Edit, View, Project, Source, Process, Simulation, Window, Help), a toolbar, and a status bar at the bottom with an '(Empty Log)' window and buttons for Console, Find in Files, Errors, and Warnings.

Select
simple
counter
tem-
plate
and
copy

Copy template to current design

The screenshot shows the Xilinx Project Navigator interface. The main window displays the VHDL code for a counter entity. The code is as follows:

```

30 entity counter is
31     Port ( clock : in std_logic;      -- vectors removed
32           direction : in std_logic;  -- vectors removed
33           count_out : out std_logic_vector(3 downto 0));
34 end counter;
35
36 architecture Behavioral of counter is
37     signal count_int : std_logic_vector(0 to 3) := "0000"; -- added
38 begin
39     process (clock)
40     begin
41         if clock='1' and clock'event then -- names replaced
42             if direction='1' then
43                 count_int <= count_int + 1;
44             else
45                 count_int <= count_int - 1;
46             end if;
47         end if;
48     end process;
49     count_out <= count_int; --added (!)
50 end Behavioral;

```

The interface also shows the 'Sources in Project' pane on the left, listing the project files, and the 'Processes for Source' pane below it, showing various design steps like 'Synthesize - XST'. The status bar at the bottom indicates 'Ln 31 Col 38 VHDL'.

Adapt
tem-
plate
as re-
quired

Adding testbench

The screenshot shows the Xilinx Project Navigator interface. A 'New Source' dialog box is open, allowing the user to create a new source file. The 'VHDL Test Bench' option is selected in the list. The 'File Name' is set to 'testbench' and the 'Location' is the project directory. The 'Add to project' checkbox is checked. The background shows the project tree with 'counter-behavioral' selected, the process view, and the console output showing compilation messages.

New Source Dialog:

- File Name: testbench
- Location: C:\marwedel\lehre\eda\05-ss\i...
- Add to project

Console Output:

```

Compiling vhdl f...
Entity <counter> compiled.
Entity <counter> (Architecture <behavioral>) compiled.

```

Add
new
source
to
counter

Set waveform for clock

Initialize Timing

Maximum output delay

Minimum input setup

Clock high for

Clock low for

Clock Timing Information
Inputs are assigned at "Input Setup Time" and outputs are checked at "Output Valid Delay".

Rising Edge Falling Edge
 Dual Edge (DDR or DET)

Clock Time High: 20 ns
Clock Time Low: 20 ns
Input Setup Time: 10 ns
Output Valid Delay: 10 ns
Initial Offset: 100 ns

Clock Information
 Single Clock: clock
 Multiple Clocks
 Combinatorial (or internal clock)

Combinatorial Timing Information
Inputs are assigned, outputs are decoded then checked. A delay between inputs and outputs avoids assignment/checking conflicts.

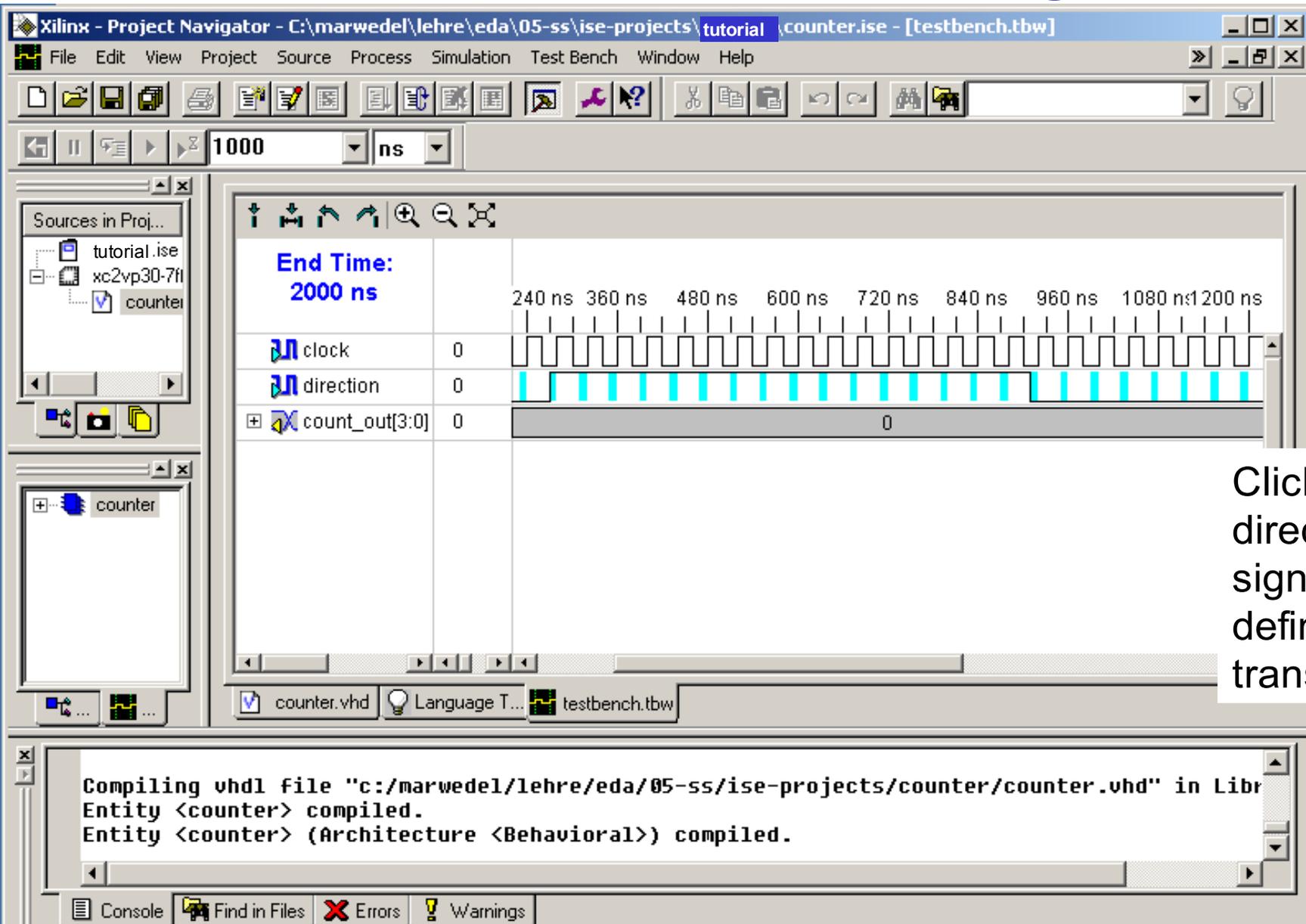
Check Outputs: 50 ns After Inputs are Assigned
Assign Inputs: 50 ns After Outputs are Checked

Global Signals
 PRLD (CPLD) GSR (FPGA)
High for Initial: 100 ns

Initial Length of Test Bench: 2000 ns
Time Scale: ns
 Add Asynchronous Signal Support

OK Cancel Next > Help

Define waveform for other signals



The screenshot displays the Xilinx Project Navigator interface. The main window shows a waveform editor for a counter circuit. The waveform is titled "End Time: 2000 ns" and shows three signals: "clock", "direction", and "count_out[3:0]". The "clock" signal is a periodic square wave. The "direction" signal is a pulse train with cyan vertical bars indicating transitions. The "count_out[3:0]" signal is a 4-bit counter output that is currently at 0. The waveform is set to a time scale of 1000 ns. The console at the bottom shows the following compilation messages:

```
Compiling vhdl file "c:/marwedel/lehre/eda/05-ss/ise-projects/counter/counter.vhd" in Libr  
Entity <counter> compiled.  
Entity <counter> (Architecture <Behavioral>) compiled.
```

Click on direction signal to define transitions

View generated testbench

The screenshot displays the Xilinx Project Navigator interface. The main window shows the source code for a testbench file named 'testbench.tbw'. The code is as follows:

```

54     PORT MAP (
55         clock => clock,
56         direction => direction,
57         count_out => count_out
58     );
59
60     PROCESS    -- clock process for clock
61     BEGIN
62         WAIT for OFFSET;
63         CLOCK_LOOP : LOOP
64             clock <= '0';
65             WAIT FOR (PERIOD - (PERIOD * DUTY_CYCLE));
66             clock <= '1';
67             WAIT FOR (PERIOD * DUTY_CYCLE);
68         END LOOP CLOCK_LOOP;
69     END PROCESS;
70
71     PROCESS

```

The left pane shows the project structure with 'Sources in Project' and 'Processes for Source: "testbench"'. The 'Processes for Source' pane lists several actions, with 'View Generated Test Bench' selected and marked with a green checkmark. The bottom pane shows the console output:

```

Entity <counter> compiled.
Entity <counter> (Architecture <Behavioral>) compiled.

```

The status bar at the bottom indicates 'Ln 1 Col 1 VHDL'.

Automatically generate expected waveform (1)

The screenshot shows the Xilinx Project Navigator interface. The 'Sources in Project' pane on the left lists the project files, with 'testbench (testbench.tbw)' circled in red. The main window displays a waveform simulation for 'count_out[3:0]' over 1000 ns. The waveform shows a clock signal and a data signal that is initially 0 and then transitions to 1. The console at the bottom shows the compilation status for the counter.vhd file.

Sources in Project:

- tutorial.isc
- xc2vp30-7ff896
- counter-behavioral (counter.vhd)
- testbench (testbench.tbw)**

Waveform Simulation:

End Time: 2000 ns

Signal	Value	Time
clock	0	0 ns
direction	0	0 ns
count_out[3:0]	0	0 ns

Console Output:

```

Compiling vhdl file "c:/marwedel/lehre/eda/05-ss/ise-projects/counter/counter.vhd" in Libr
Entity <counter> compiled.
Entity <counter> (Architecture <Behavioral>) compiled.
  
```

Select
testbench
and check
process
view

Automatically generate expected waveform (2)

The screenshot shows the Xilinx ISE Project Navigator interface. The main window displays the source code for 'testbench.vhw'. The 'Processes for Source' pane on the left shows the 'Generate Expected Simulation Results' option highlighted. The console at the bottom shows the command and design name.

File Edit View Project Source Process Simulation Window Help

1000 ns

Sources in Project:

- tutorial.ise
- xc2vp30-7ff896
- counter-behavioral (counter.vhd)
 - testbench (testbench.tbw)

Processes for Source: "testbench"

- Add Test Bench To Project
- Xilinx ISE Simulator
 - Generate Expected Simulation Results
 - Simulate Behavioral Model
 - Simulate Post-Place

```

1
2  -- Copyright (c) 1995-2003 Xilinx, Inc.
3  -- All Right Reserved.
4
5  --
6  --
7  --
8  -- Vendor: Xilinx
9  -- Version : 7.1i
10 -- Application : ISE Foundation
11 -- Filename : testbench.vhw
12 -- Timestamp : Sat May 07 17:02:56 2005
13
14 --
15 -- Command:
16 -- Design Name: testbench
17 -- Device: Xilinx

```

Design Sum... counter.vhd Language T... testbench.tbw testbench.vh...

Console Find in Files Errors Warnings

Hierarchy is up to date.

Ln 1 Col 1 VHDL

Requires ISE to be specified as the simulator for the project (and simulator must be available).

Replacing the original testbench

Over-
writing
initial
test-
bench

The screenshot shows the Xilinx Project Navigator interface. The main window displays the source files for the project, including the testbench (testbench.tbw). A dialog box titled "Test Bench Waveform Editor" is open, asking: "Only one instance of testbench.tbw can be active at once. Would you like to close the current testbench.tbw and open a new one?" with buttons for "Ja", "Nein", and "Abbrechen".

The console window at the bottom shows the following error message:

```
Simulation stopped when executing process: testbench.ant:104
on line 122 in file "C:/marwedel/lehre/eda/05-ss/ise-projects/tutorial/testbench.ant"
```

The status bar at the bottom indicates: "Process 'Generate Expected Simulation Results' is up to date." and shows the current file as "testbench.tbw".

Automatic or manual comparison ?

The screenshot shows the Xilinx Project Navigator interface. The top menu bar includes File, Edit, View, Project, Source, Process, Simulation, Test Bench, Window, and Help. Below the menu is a toolbar with various icons. The main workspace is divided into several panes:

- Sources in Project:** A tree view showing the project structure, including tutorial.isc, xc2vp30-7ff896, counter-behavioral (counter.vhd), and testbench (testbench.tbw).
- Waveform:** A timing diagram showing signals over time. The end time is 2000 ns. The signals shown are clock (0), direction (1), and counter_out[...]. The counter_out signal is currently at 13.
- Expected Results:** A dialog box with the text: "Replace outputs with expected values? Selecting 'No' adds the expected values as signals to the display for comparison." The dialog has three buttons: Ja, Nein, and Abbrechen.
- Console:** A text area at the bottom showing compilation messages: "Compiling vhdl file 'c:/marwedel/lehre/eda/05-ss/ise-projects/tutorial/counter.vhd' in...", "Entity <counter> compiled.", and "Entity <counter> (Architecture <Behavioral>) compiled."

A red arrow points from the text box on the right to the 'Expected Results' dialog box.

Click on
yes/Ja
in order
to
compare
auto-
mati-
cally.
Initially
un-
known.

Automatic comparison

The screenshot shows the Xilinx Project Navigator interface. The main window displays a simulation waveform for a counter. The waveform includes a clock signal, a direction signal, and a counter output signal. The counter output is highlighted with a red oval and an arrow pointing to the text "Added when responding 'yes' for the 1st time".

The simulation parameters are set to 1000 ns. The end time is 2000 ns. The counter output is shown as a series of pulses, with the first pulse highlighted in red.

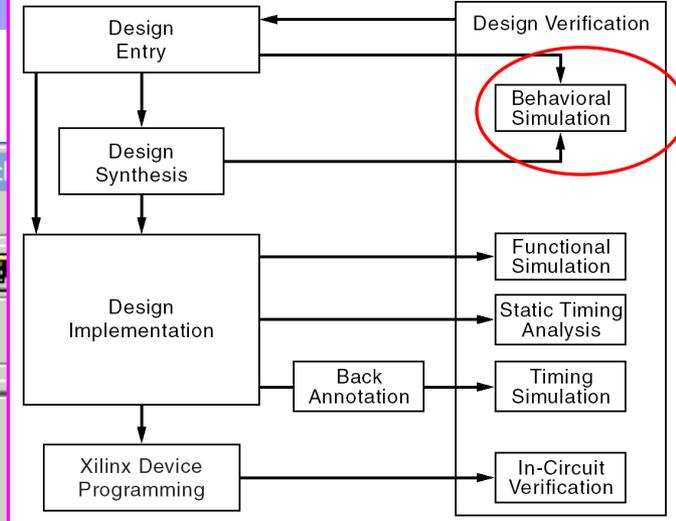
The console window at the bottom shows the compilation results:

```

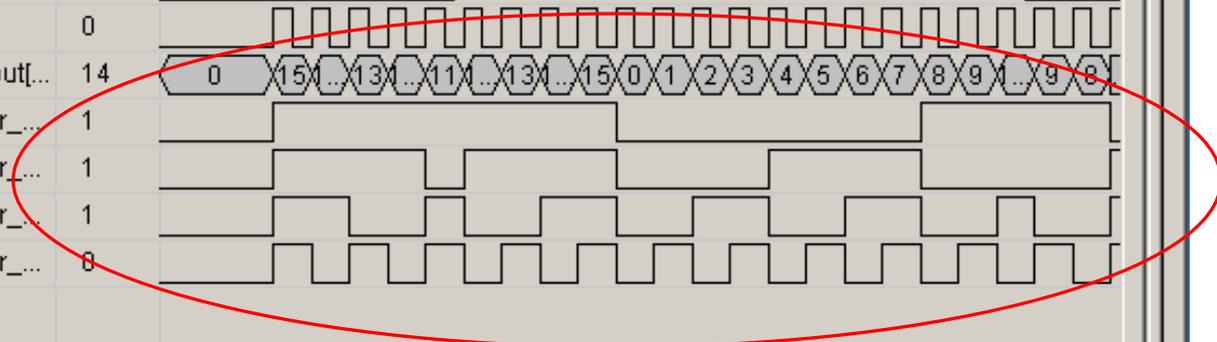
Compiling vhdl file "c:/marwedel/lehre/eda/05-ss/ise-projects/tutorial/counter.vhd" in Lit
Entity <counter> compiled.
Entity <counter> (Architecture <Behavioral>) compiled.
  
```

Added
when
responding
'yes' for the
1st time

Behavioral simulation



The screenshot shows the Xilinx Project Navigator interface. The main window displays a timing diagram for a simulation. The time scale is in nanoseconds (ns), with markers at 0 ns, 202 ns, and 404 ns. The simulation is currently stopped at 2040 ns. The waveform shows several signals: 'direction' (a step function), 'clock' (a periodic square wave), and a counter output 'counter_out[...]' which displays a sequence of values: 0, 15, 13, 11, 13, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 9, 8. Other signals include 'counter_...' (multiple instances) showing various digital waveforms.



Simulation stopped when executing process: testbench.vhw:69
 on line 108 in file "C:/marwedel/lehre/eda/05-ss/ise-projects/tutorial/testbench.vhw"

Console Find in Files Errors Warnings Sim Console

Adding timing constraints (1)

The screenshot displays the Xilinx Project Navigator interface. The 'Processes for Source: "counter-b...' window is open, showing a list of actions. The 'Create Timing Constraints' option is highlighted with a red circle. The main window shows a timing diagram with a 'Now: 2040 ns' label. The console at the bottom shows an error message: 'Simulation stopped when executing process: testbench.vhw:69 on line 108 in file "C:/marwedel/lehre/eda/05-ss/ise-projects/tutorial/testbench.vhw"'.

Simulation stopped when executing process: testbench.vhw:69
on line 108 in file "C:/marwedel/lehre/eda/05-ss/ise-projects/tutorial/testbench.vhw"

Double
click on
timing
con-
straints

Adding timing constraints (2)

The screenshot shows the Xilinx Project Navigator interface. The main window displays a timing diagram for a signal named 'direction'. The current time is 2040 ns. The diagram shows a square wave signal with a period of 202 ns. The signal is high from 0 ns to 202 ns, low from 202 ns to 404 ns, and high again from 404 ns to 606 ns. The signal is then low from 606 ns to 808 ns, and high from 808 ns to 1010 ns. The signal is labeled with values 5, 6, 7, 8, 9, 9, 8.

A dialog box titled 'Xilinx Project Navigator' is open, asking: 'This process requires that an Implementation Constraint File (UCF) be added to the project and associated with the selected design module. Would you like Project Navigator to automatically create a UCF and add it to the project at this time? If you select "No" you will need to create or add an existing UCF to the project before running this process.' The dialog has 'Ja' and 'Nein' buttons.

The 'Processes for Source' pane shows a context menu for 'counter-behavioral (counter.vhd)'. The menu items are: View Hierarchy, User Constraints, Create Timing Constraints (highlighted), Assign Package Footprint, Create Area Constraints, Edit Constraints (1), and Synthesize - XST.

The bottom status bar shows the process 'Create Timing Constraints' is up to date.

Adding timing constraints (3)

The screenshot shows the Xilinx Project Navigator interface with the Xilinx Constraints Editor open. The editor displays a table of timing constraints for the 'clock' net. The table has four columns: Clock Net Name, Period, Pad to Setup, and Clock to Pad. The 'clock' net is listed with a period of 40 ns HIGH 50 %, a pad to setup of 10 ns, and a clock to pad of 10 ns. The '40 ns HIGH 50 %' value is circled in red. Below the table, the Global tab is selected, showing the following constraints:

```

NET "clock" TNM_NET = "clock";
TIMESPEC "TS_clock" = PERIOD "clock" 40 ns HIGH 50 %;
OFFSET = IN 10 ns BEFORE "clock" ;
OFFSET = OUT 10 ns AFTER "clock" ;

```

The background shows a timing diagram for the clock signal, with a period of 40 ns and a high time of 20 ns (50% duty cycle). The clock signal is shown as a square wave with a period of 40 ns and a high time of 20 ns. The diagram also shows the clock signal connected to a counter circuit, with the counter output showing a sequence of numbers 7, 8, 9, 0, 9, 8.

Add pin constraints

Use
table
from
slides
fga-01

Xilinx PACE - C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\counter.ucf

File Edit View IOBs Areas Tools Window Help

Loading device for application Rf. Device from file '2vp30.nph' in environment C:\Programme\xilinx.

Design Browser

- I/O Pins
- Global Logic
- Logic

Design Object List - I/O Pins

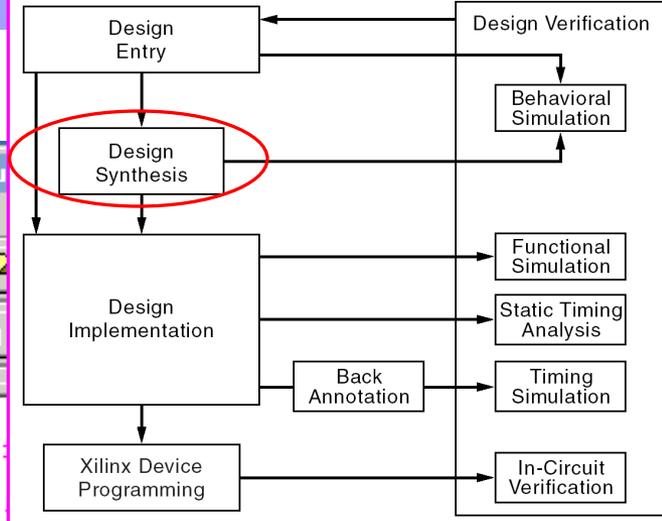
I/O Name	Loc	Bank	I/O Std.	Vref	Vcc
clock	AG5	BANK3	LVTTL	N/A	3.3
counter_out<0>	AC4	BANK3	LVTTL	N/A	3.3
counter_out<1>	AC3	BANK3	LVTTL	N/A	3.3
counter_out<2>	AA6	BANK3	LVTTL	N/A	3.3
counter_out<3>	AA5	BANK3	LVTTL	N/A	3.3
direction	AC11	BANK4	LVTTL	N/A	2.5

Package Pins for xc2vp30-7-ff896

Top View

Package View Architecture View

Synthesis



Xilinx - Project Navigator - C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\tutorial.ise - [C...]

File Edit View Project Source Process Simulation Window Help

1000 ns

Sources in Project:

- tutorial.ise
- xc2vp30-7ff896
 - counter-behavioral (counter.vhd)
 - testbench (testbench.tbw)
 - counter.ucf

Processes for Source: "counter-behavi..."

- Create Area Constraint
- Edit Constraints (Text)
- Synthesize - XST**
- View Synthesis Report
- View RTL Schematic
- View Technology Sch
- Check Syntax
- Generate Post-Synthe
- Post-Synthesis
- Implement Design
- Translate

```

30 entity counter is
31     Port ( direction : in std_log;
32           clock : in std_logic;
33           counter_out : out std_
34 end counter;
35
36 architecture Behavioral of counter is
37     signal counter_int : std_logic_vector(3 downto 0) := "0000";
38 begin
39     process (clock)
40     begin
41         if clock='1' and clock'event then
42             if direction='1' then
43                 counter_int <= counter_int + 1;
44             else
45                 counter_int <= counter_int - 1;
46             end if;
47         end if;
48     end process;
49     counter_out <= counter_int; --added
50 end Behavioral;
51
    
```

Process View Hierarchy - test...

Console Find in Files Errors Warnings

Hierarchy is up to date.

Ln 47 Col 12 VHDL

Viewing synthesis results (1)

The screenshot shows the Xilinx Project Navigator interface. The main window displays the VHDL code for an entity named 'counter'. The code is as follows:

```

30 entity counter is
31     Port ( direction : in std_logic;
32           clock      : in std_logic;
33           counter_out : out std_logic_vector(3 downto 0) )
34 end counter;
35
36 architecture Behavioral of counter is
37     signal counter_int : std_logic_vector(3 downto 0) := "0000";
38 begin
39     process (clock)
40     begin
41         if clock='1' and clock'event then
42             if direction='1' then
43                 counter_int <= counter_int + 1;
44             else
45                 counter_int <= counter_int - 1;
46             end if;
47         end if;
48     end process;
49     counter_out <= counter_int; --added
50 end Behavioral;
51

```

In the 'Processes for Source' pane, the 'Synthesize - XST' process is highlighted with a red circle. The 'View RTL Schematic' option is also visible in the same pane.

On the right side of the image, the text "Double click on view RTL" is written, indicating the action to be taken.

Double
click on
view
RTL

Viewing synthesis results (2)

The screenshot shows the Xilinx Project Navigator interface. The main window displays the top-level symbol for the counter module, which is a rectangular box containing the text "clock counter_out(3:0)" and "direction". A blue line points from the text "Initially, top level module is visible." to the "clock counter_out(3:0)" text. The interface includes a menu bar (File, Edit, View, Project, Source, Process, Simulation, Window, Help), a toolbar with various icons, and several panels. The "Instance Contents" panel on the left shows a tree view with "Pins", "Nets", and "Instances". The "Select the Modules or Snapshot tab" panel below it shows "(No Processes Available)". The bottom status bar shows the current project name "counter.ngr" and the coordinates "[155,161]".

clock counter_out(3:0)

direction

Top Level Symbol

Initially, top level module is visible.

© Xilinx,
P. Marwedel

Enter lower level of the hierarchy (1)

The screenshot shows the Xilinx Project Navigator interface. The main window displays a schematic diagram with a context menu open over the signal `counter_out(3:0)`. The menu options are:

- Zoom
- Select Object(s)
- Refresh (F5)
- Find
- Regenerate Schematic
- Synchronize Windows
- Add Name
- Delete Name
- Pop to the Calling Schematic
- Push Into the Selected Instance**
- Open Source of Selected Instance
- Open All Hdl Source Files
- Show Sheets of Selected Nets...
- Show Lut Content
- Object Properties...
- Back a Schematic
- Forward a Schematic
- List of Schematics...

The signal name `counter_out(3:0)` and the word `direction` are highlighted with a red box. A red line points from the text 'Right click on module' to the signal name.

Right
click on
module

Enter lower level of the hierarchy (2)

The screenshot shows the Xilinx Project Navigator interface. The main workspace displays a circuit diagram with the following components and connections:

- An input labeled "Up Down" is connected to a component labeled "UpDown" with instance name "_n000".
- The output of "UpDown" is connected to the "Data[3:0]" input of a component labeled "AddSub".
- The output of "AddSub" is connected to the "Data[3:0]" input of a flip-flop component labeled "FD".
- The output of "FD" is connected to the "Data[3:0]" input of "AddSub", forming a feedback loop.
- An input labeled "Clk" is connected to the clock input "c" of the "FD" flip-flop.
- The output of "FD" is connected to a 4-bit bus labeled "Q[3:0]".

A tooltip for the "FD" component is visible, showing the following details:

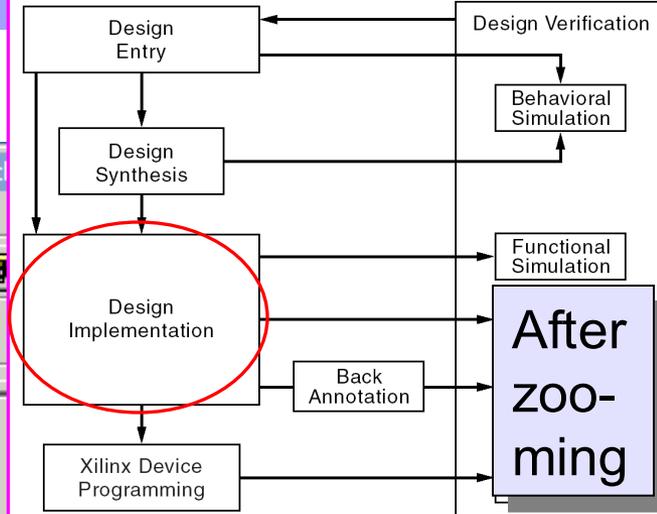
```

Instance = 3,2,1,0
Type = fd
-----
Input : C => Clk
Input : D => _n0000(3:0)
Output : Q => Q(3:0)
  
```

The left sidebar shows the "Instance Contents" tree with "Mad" expanded to "_n00" and "3,2,1". The "Select the Module..." window is empty, showing "(No Processes Availa)". The bottom status bar shows the current design is "Ready" and the coordinates are "[1509,422]".

Oops: no counter register, but separate add/sub component; Additional buffers generated

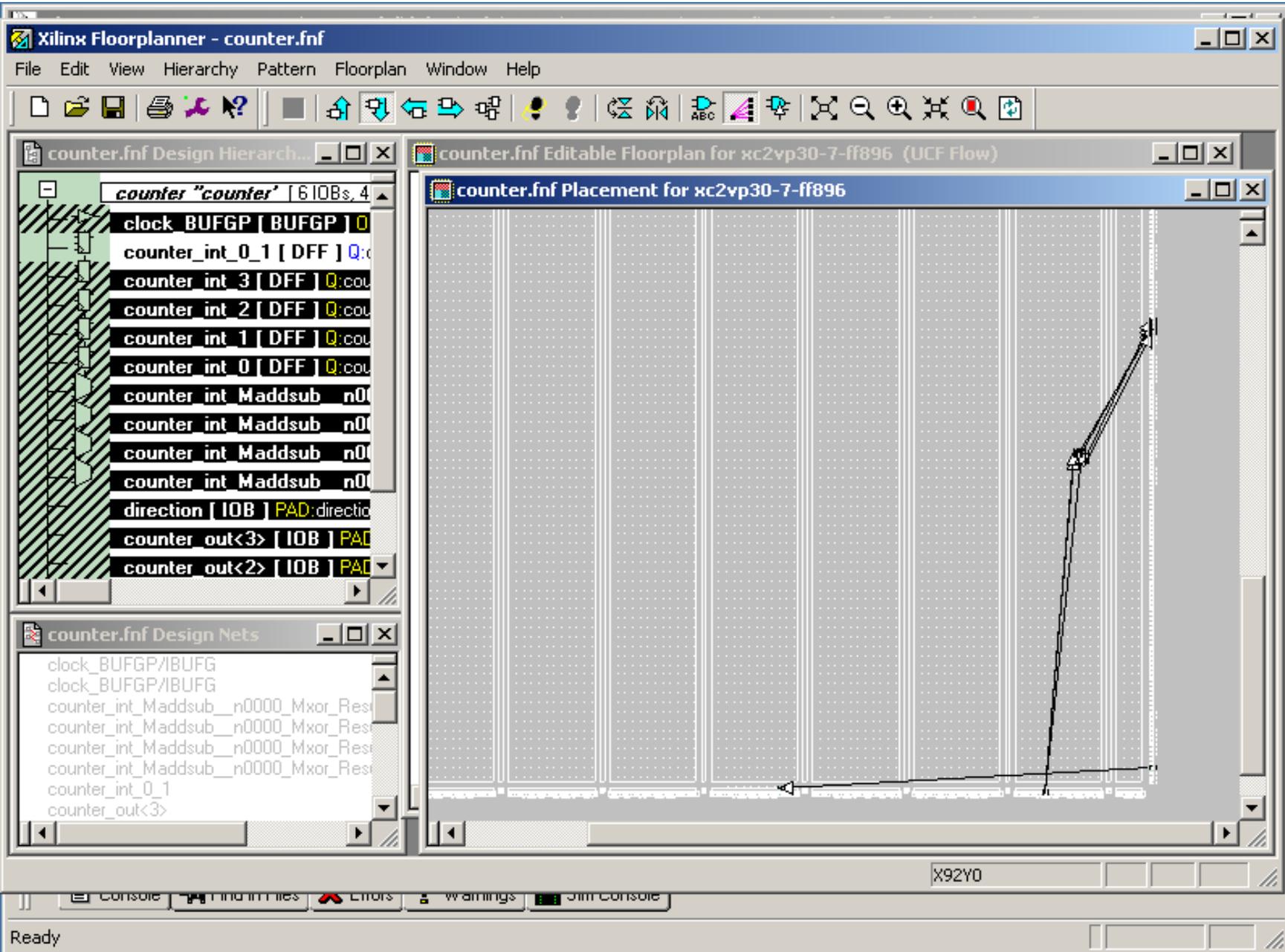
After placement & routing



Signal	Value
direction	1
clock	0
counter_out[...]	14
counter_...	1
counter_...	1
counter_...	1
counter_...	0

After double click on place & route; now: check result

View result of placement and routing (1)



After
ZOO-
ming

View result of placement and routing (2)

The screenshot shows the Xilinx Floorplanner interface for a design named 'counter.fnf'. The main window displays the 'Placement' view for the device 'xc2vp30-7-ff896'. The design hierarchy on the left lists components such as 'clock_BUFPG', 'counter_int_0_1', 'counter_int_3', 'counter_int_2', 'counter_int_1', 'counter_int_0', and several 'counter_int Maddsub' blocks. The 'Design Nets' window at the bottom left lists nets like 'clock_BUFPG/IBUFG' and 'counter_int_Maddsub_n0000_Mxor_Res'. The main floorplan area shows a grid with a component labeled 'X88Y46' and routing paths connecting to pins AA5, AA6, AC3, and AC4 on the right side of the device. A red circle highlights these connections. The status bar at the bottom shows 'X88Y53'.

After zooming even more

List of used components

Xilinx Floorplanner - counter.fnf

File Edit View Hierarchy Pattern Floorplan Window Help

counter.fnf Design Hierarchy

```

counter "counter" [ 6 IOBs, 4 FGs, 5 DFFs, 1 BUFG ]
clock_BUFPG [ BUFG ] D:clock_BUFPG I:clock
counter_int_0_1 [ DFF ] Q:counter_int_0_1 D:N6 R:counter_int<0> C:clock_BUFPG
counter_int_3 [ DFF ] Q:counter_int<3> D:counter_int_n0000<3> C:clock_BUFPG
counter_int_2 [ DFF ] Q:counter_int<2> D:counter_int_n0000<2> C:clock_BUFPG
counter_int_1 [ DFF ] Q:counter_int<1> D:counter_int_n0000<1> C:clock_BUFPG
counter_int_0 [ DFF ] Q:counter_int<0> D:N6 R:counter_int<0> C:clock_BUFPG
counter_int_Maddsub_n0000_Mxor_Result<3>_Xo<1>1_SW0 [ FG ] O:counter_int_Maddsub_
counter_int_Maddsub_n0000_Mxor_Result<3>_Xo<1>1 [ FG ] O:counter_int_Maddsub_n0000_
counter_int_Maddsub_n0000_Mxor_Result<2>_Xo<1>1 [ FG ] O:counter_int_Maddsub_n0000_
counter_int_Maddsub_n0000_Mxor_Result<1>_Xo<1>1 [ FG ] O:counter_int_Maddsub_n0000_
direction [ IOB ] PAD:direction I:direction_IBUF
counter_out<3> [ IOB ] PAD:counter_out<3> O1:counter_int<3>
counter_out<2> [ IOB ] PAD:counter_out<2> O1:counter_int<2>
counter_out<1> [ IOB ] PAD:counter_out<1> O1:counter_int<1>
counter_out<0> [ IOB ] PAD:counter_out<0> OTCLK1:clock_BUFPG SR:counter_int<0>
clock [ IOB ] PAD:clock I:clock_BUFPG/IBUFG
  
```

W8
AB3
AB4
AB2
AC2
AAS
AA6
AC3
AC4
AD1
AD2
Y7
Y8
AB5
AB6
AE1
AC5

X79Y45

Console Find in files Errors warnings Jim Console

Ready

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Viewing the design summary

Xilinx - Project Navigator - C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\tutorial.ise - [Design Summary]

File Edit View Project Source Process Simulation Window Help

Sources in Project:

- tutorial.ise
- xc2vp30-7ff896
- counter-behavioral (counter.vh)**
- testbench (testbench.tbw)
- counter.ucf

Processes for Source: "counter-beh..."

- Create New Source
- View Design Summary**
- Design Utilities
 - Create Schematic Syn
 - View Command Line I
 - Check Syntax for Sim
 - Launch Xilinx ISE Sim
 - View HDL Instantiation
- User Constraints
 - Create Timing Constr
 - Assign Package Pins

Design Overview for counter

Property	Value
Project Name:	c:\marwedel\lehre\eda\05-ss\ise-projects\tutorial
Target Device:	xc2vp30
Constraints File:	counter.ucf
Report Generated:	Saturday 05/07/05 at 17:48
Printable Summary (View as HTML)	counter_summary.html

Device Utilization Summary

Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops:	4	27,392	1%	
Number of 4 input LUTs:	4	27,392	1%	
Logic Distribution:				
Number of occupied Slices:	3	13,696	1%	
Number of Slices containing only related logic:	3	3	100%	
Number of Slices containing unrelated logic:	0	3	0%	
Total Number 4 input LUTs:	4	27,392	1%	
Number of bonded IOBs:	6	556	1%	
Number of PPC405s:	0	2	0%	
Number of GCLKs:	1	16	6%	
Number of GTs:	0	8	0%	
Number of GT10s:	0	0	0%	

Performance Summary

Design Sum... counter.vhd Language ... testbench... testbench... testbench_...

Console Find in Files Errors Warnings Sim Console

Estimated power consumption

Xilinx XPower - [counter.pwr]

File Edit View Tools Window Help

	Voltage	Current	Power
Dyna		0.00	0.00
Quies		167.00	417.50
Vcco3	3.3		
Dyna		0.00	0.00
Quies		1.25	4.13

Su... Pow... Curr... The...

Power summary:

	I (mA)	P (mW)

Total estimated power consumption:		500

Vccint 1.50V:	50	75
Vccaux 2.50V:	167	418
Vcco33 3.30V:	1	4
Vcco25 2.50V:	1	3

Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0

Quiescent Vccint 1.50V:	50	75

WARNING: Power:410 - No thermal characteristics available for this device / package combination.
 XPower and Datasheet may have some Quiescent Current differences.
 This is due to the fact that the quiescent numbers in XPower are based on measurements of real designs with active functional elements reflecting real world design scenarios.

For Help, press F1

2vp30ff896-7

Generate Post-Place & Route Static Timing

Sources in Project:

- tutorial.ise
- xc2vp30-7ff896
 - counter-behavioral (counter.vhd)
 - testbench (testbench.tbw)
 - counter.ucf

Processes for Source: "counter-behavioral"

- Map
- Place & Route
 - Place & Route Report
 - Asynchronous Delay Report
 - Pad Report
 - Guide Results Report
 - Generate Post-Place & Route Static Timing**
 - Post-Place & Route Static Timing Report
 - Text-based Post-Place & Route Static Timir
 - Generate Primetime Netlist
 - Analyze Post-Place & Route Static Timing

Performance Summary

Property	Value
Final Timing Score:	0
Number of Unrouted Signals:	All signals are completely routed.
Number of Failing Constraints:	0

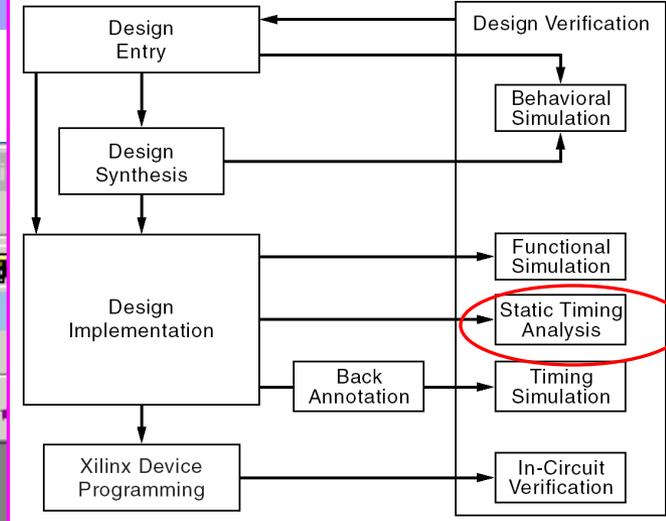
Failing Constraints

Constraint(s)	Requested	Actual	Logic Levels
All Constraints Met			

Detailed Reports

Report Name	Status	Last Date Modi
Synthesis Report	Current	Saturday 05/07/0
Translation Report	Current	Saturday 05/07/0
Map Report	Current	Saturday 05/07/0
Pad Report	Current	Saturday 05/07/0
Place and Route Report	Current	Saturday 05/07/0
Post Place and Route Static Timing Report	Current	Saturday 05/07/0

Checking Timing constraints (1)



Xilinx - Project Navigator - C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\tutorial.ise - [Desi

File Edit View Project Source Process Simulation Window Help

Xilinx Timing Analyzer - counter.ncd

File Edit View Analyze Window Help

Against Timing Constraints...
 Against Auto Generated Design Constraints...
 Against User Specified Paths
 Constraints Interaction...
 Query Nets...
 Query Timegroups...
 Reset All Path Filters

```

    1 >OpenDesign NoDefaultPCF C:\marwedel\lehre\eda\05-ss\ise-projects\
    Loading device for application RF_Device from file '2vp30.nph' in en
    "counter" is an NCD, version 3.1, device xc2vp30, package ff896,
    2 >OpenPCF C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\counter
    
```

Perform a timing constraints analysis, reporting on all paths covered by timi C:\marwedel\lehre\eda\05-ss\ise-projects\

Console Find in Files Errors Warnings Sim Console

completely routed.

ic Levels

st Date Modi
aturday 05/07/0

testb... testb...

Checking Timing constraints (2)

The screenshot shows the Xilinx Timing Analyzer interface. The main window displays the 'Timing Constraints Analysis Report 1'. The left-hand pane shows a tree view of the report contents, with 'Data Sheet report' and its sub-item 'Timing summary' highlighted by a red circle. The main text area shows the following report content:

```

Timing Report Description
+ INFO Messages
+ Timing Constraints
  Constraint compliance
+ Data Sheet report:
  Timing summary
Timing Analyzer Settings:

Timing summary
-----
Timing errors: 0   Score: 0

Constraints cover 18 paths, 0 nets, and 26 connections

-----Footnotes-----
1) The minimum period statistic assumes all single cycle

Analysis completed Sat May 07 18:27:06 2005
-----

Timing Analyzer Settings:
-----
OpenPCF C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\count
Speed -7
IncludeNets
  
```

The bottom status bar shows the command window with the following text:

```

1 >OpenDesign NoDefaultPCF C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\count
Loading device for application Rf_Device from file '2vp30.nph' in environment C:/P
"counter" is an NCD, version 3.1, device xc2vp30, package ff896, speed -7
  
```

The status bar also includes tabs for 'Output', 'Error', 'Warning', and 'Command', and a path indicator: C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\count

View routed design (1)

The screenshot shows the Xilinx Project Navigator interface. The top menu bar includes File, Edit, View, Project, Source, Process, Simulation, Window, and Help. The toolbar contains various icons for file operations and simulation. The 'Sources in Project' pane on the left shows the project structure for 'tutorial.isc', including 'counter-behavioral (counter.vhd)', 'testbench (testbench.tbw)', and 'counter.ucf'. The 'Processes for Source: "counter-behavioral"' pane is open, and the 'View/Edit Routed Design (FPGA Editor)' process is highlighted with a red circle. The main window displays a simulation waveform for 'testbench_isim' with a time scale of 1000 ns. The waveform shows signals for 'direction', 'clock', 'counter_out...', and 'counter_...'. The 'counter_out...' signal is highlighted with a red circle. The 'Process View' pane at the bottom shows 'Sim Hierarchy - testbench_isim'.

File Edit View Project Source Process Simulation Window Help

Sources in Project:

- tutorial.isc
 - xc2vp30-7ff896
 - counter-behavioral (counter.vhd)
 - testbench (testbench.tbw)
 - counter.ucf

Module View Snapshot View Library View

Processes for Source: "counter-behavioral"

- Generate Primetime Netlist
- Analyze Post-Place & Route Static Timing (FPGA Editor)
- View/Edit Placed Design (Floorplanner)
- View/Edit Routed Design (FPGA Editor)
- Analyze Power (XPower)
- Generate Power Data
- Generate Post-Place & Route Simulation Model
- Generate IBIS Model
- Multi Pass Place & Route
- Back-annotate Pin Locations
- Generate Programming File

Process View Sim Hierarchy - testbench_isim

testbench.tbw

testbench_isim

Now: 2040 ns

0 ns 202 404 ns

direction	1	
clock	0	
counter_out...	14	0
counter_...	1	

10 -- / / Filename

counter... Langua... testben... testben... testbenc...

Console Find in Files Errors Warnings Sim Console

View routed design (2)

The screenshot shows the Xilinx FPGA Editor interface. The 'View' menu is open, and 'Zoom Selection F11' is highlighted. The 'List1' window displays a table of components:

	Name	Site	Type	#Pi	Hilite
1	clock	AG5	IOB	1	no c
2	clock_BUFGRP/B	BUFGMU	BUFG	3	no c
4	counter_int<0>	SLICE_X8	SLICE	4	no c
4	counter_int<2>	SLICE_X8	SLICE	14	no c
5	counter_int<3>	SLICE_X8	SLICE	11	no c
6	counter_out<0>	AC4	IOB	3	no c
7	counter_out<1>	AC3	IOB	1	no c
8	counter_out<2>	AA6	IOB	1	no c

The status bar at the bottom reads: "Adjusts the scale of the current view so that the selected objects can be seen in the window".

View routed design (3)

Xilinx FPGA Editor - counter.ncd

File Edit View Tools Window Help

Array1

List1

All Components

Name Filter

*

Apply

	Name	Site	Type	#Pi	Hilite
1	clock	AG5	IOB	1	no cl
2	clock_BUFGP/B	BUFGMU	BUFG	3	no cl
3	counter_int<0>	SLICE_X8	SLICE	4	no cl
4	counter_int<2>	SLICE_X8	SLICE	14	no cl
5	counter_int<3>	SLICE_X8	SLICE	11	no cl
6	counter_out<0>	AC4	IOB	3	no cl
7	counter_out<1>	AC3	IOB	1	no cl
8	counter_out<2>	AA6	IOB	1	no cl

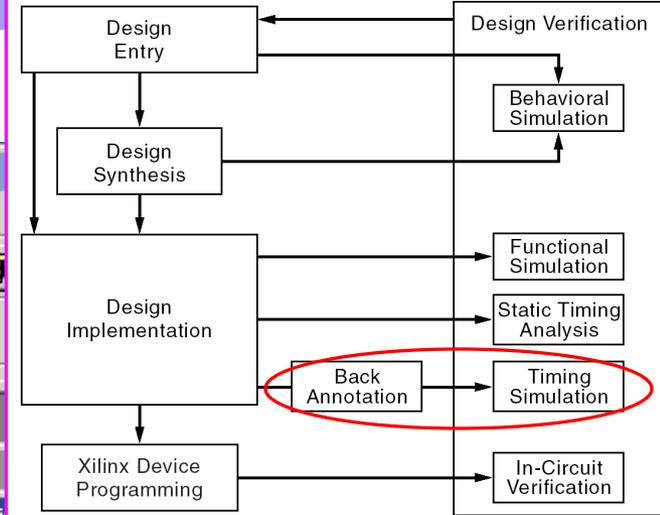
World1

Loading speed info...

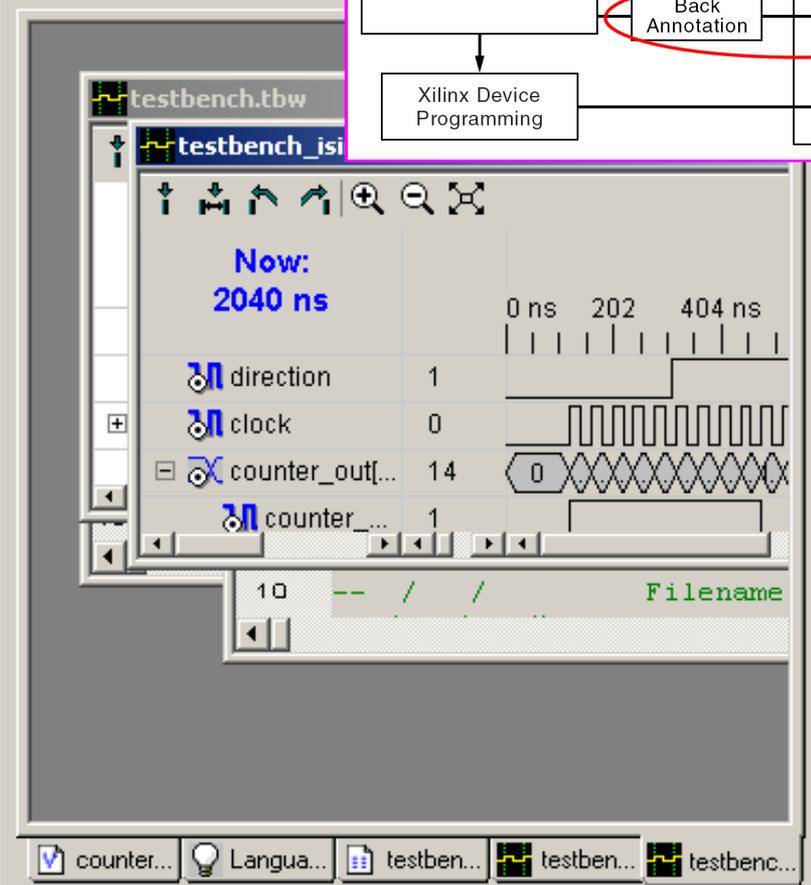
xc2vp30-7ff896 No Logic Changes

4
slices
in 1
CLB
used

Simulate Post-Place & Route HDL Model (1)



The screenshot shows the Xilinx Project Navigator interface. The top menu bar includes File, Edit, View, Project, Source, Process, Simulation, Window, and Help. Below the menu is a toolbar with various icons. A simulation control bar shows a play button, a pause button, and a time counter set to 1000 ns. The 'Sources in Project' pane on the left shows a tree view with 'tutorial.ise' at the root, containing 'xc2vp30-7ff896', 'counter-behavioral (counter.vhd)', 'testbench (testbench.tbw)', and 'counter.ucf'. The 'Processes for Source: "testbench"' pane shows a list of actions, with 'Simulate Post-Place & Route HDL Model' circled in red. Other actions include 'Add Existing Source', 'Create New Source', 'View Generated Test Bench As HDL', 'Add Test Bench To Project', and 'Xilinx ISE Simulator'.



Simulate Post-Place & Route HDL Model (2)

Xilinx - Project Navigator - C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\tutorial.ise - [testbench_ism]

File Edit View Project Source Process Simulation Test Bench Window Help

1000 ns

Sources in Project:

- tutorial.ise
- xc2vp30-7ff896
 - counter-behav
 - testbench
 - counter.u

Now: 2040 ns

113 ns 119 125 ns 132 138 ns 144

direction	1					
clock	0					
counter_out[...]	14	0	1	15		
counter_...	1					
counter_...	1					
counter_...	1					
counter_...	0					

Proc... Sim H...

counter.vhd Language T... testbench.v... testbench.tbw testbench_ism

Console Find in Files Errors Warnings Sim Console

Propagation delays are visible at this level

Simulate Post-Place & Route HDL Model (3)

Xilinx - Project Navigator - C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\tutorial.ise - [testbench_ism]

File Edit View Project Source Process Simulation Test Bench Window Help

1000 ns

Sources in Project:

- tutorial.ise
- xc2vp30-7ff896
- counter-behav
- testbench
- counter.u

testbench testbench

Now: 2040 ns

113 ns 119 125 ns 132 138 ns 144

119.9 128.3

8.4 ns

direction 0

clock 1

counter_out[...] 5 0 1 15

counter_... 0

counter_... 1

counter_... 0

counter_... 1

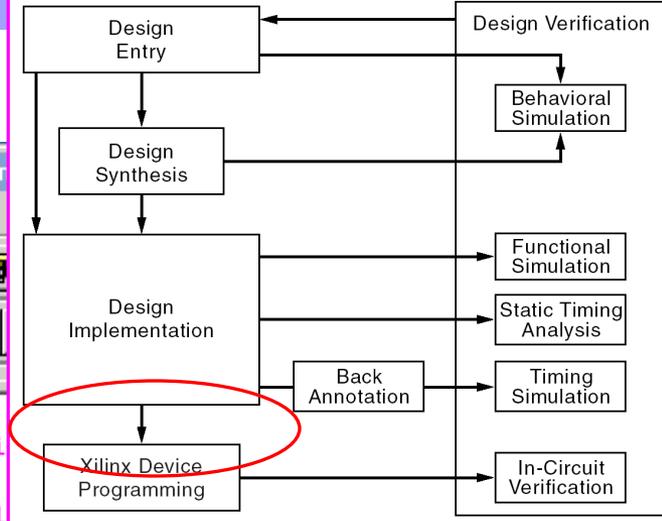
counter.vhd Language T... testbench.v... testbench.tbw testbench_ism

Proc... Sim H...

Console Find in Files Errors Warnings Sim Console

Using the
measure
marker

Generation of configuration file



Xilinx - Project Navigator - C:\marwedel\lehre\eda\05-ss\ise-projects\tutorial\tutorial.ise - [c...

File Edit View Project Source Process Simulation Window Help

1000 ns

Sources in Project:

- tutorial.ise
- xc2vp30-7ff896
 - counter-behavioral (counter.vh)
 - testbench (testbench.tbw)
 - counter.ucf

Processes for Source: "counter-behavi..."

- Analyze Power
- Generate Power
- Generate Post-I
- Generate IBIS P
- Multi Pass Plac
- Back-annotate
- Generate Programming File
- Programming File Gen
- Generate PROM, ACE
- Configure Device (IMF)

```

30 entity counter is
31     Port ( direction : in std_logic;
32           clock : in std_logic;
33           counter_out : out std_logic)
34 end counter;
35
36 architecture Behavioral of counter is
37     signal counter_int : std_logic_vector(3 downto 0) := "0000";
38 begin
39     process (clock)
40     begin
41         if clock='1' and clock'event then
42             if direction='1' then
43                 counter_int <= counter_int + 1;
44             else
45                 counter_int <= counter_int - 1;
46             end if;
47         end if;
48     end process;
49     counter_out <= counter_int; --added
50 end Behavioral;
51
    
```

counter.vhd Language T... testbench.v... testbench.tbw

Generation of configuration file

The screenshot shows the Xilinx Project Navigator interface. The 'Sources in Project' pane on the left shows the project structure, including the 'counter-behavioral' source. The 'Processes for Source' pane shows the 'Generate Programming File' process as completed. The console window displays the following output:

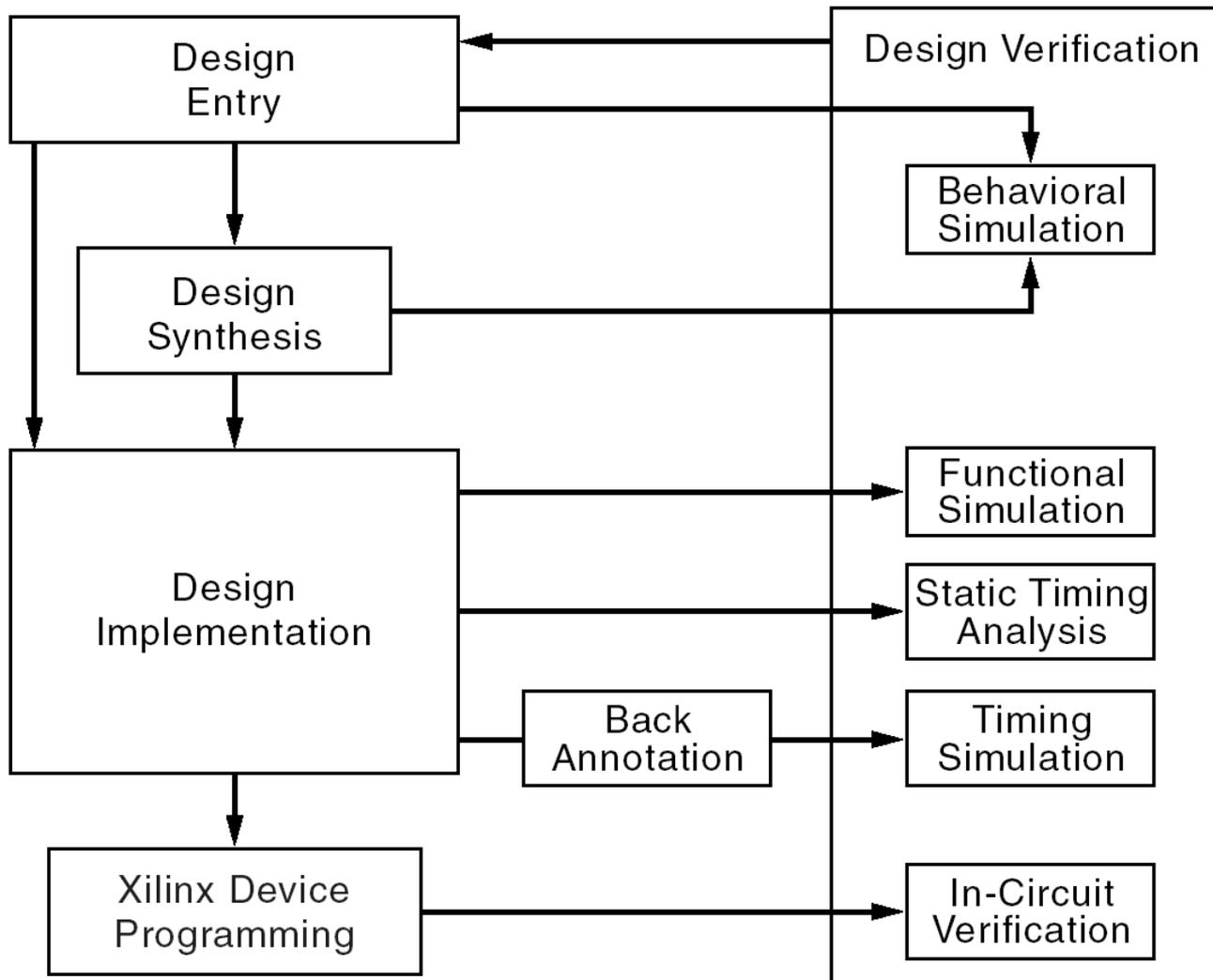
```

119 +-----+-----+
120 | KeyFile           | (Not Specified) * |
121 +-----+-----+
122 | StartKey         | 0*                 |
123 +-----+-----+
124 | StartCBC         | pick*              |
125 +-----+-----+
126 | FreezeDCI        | No*                 |
127 +-----+-----+
128 | DCIUpdateMode    | AsRequired**       |
129 +-----+-----+
130 | IEEE1532         | No*                 |
131 +-----+-----+
132 | Binary           | No**                |
133 +-----+-----+
134 * Default setting.
135 ** The specified setting matches the default setting.
136
137 Running DRC.
138 DRC detected 0 errors and 0 warnings.
139 Creating bit map...
140 Saving bit stream in "counter.bit".

```

The final three lines of the console output (137-140) are circled in red, indicating the successful completion of the configuration file generation process.

Summary



Fast path through design flow with Xilinx ISE