FPGA Synthesis
Different specification techniques

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Gliederung

Zeitplan

- **Einführung**
- **SystemC**
  - Vorlesungen und Programmierung

3,5 Wochen

→ **FPGAs**
  - Vorlesungen
  - VHDL-basierte Konfiguration von FPGAs mit dem XUP VII Pro Entwicklungssystem

3,5 Wochen

- **Algorithmen**
  - Mikroarchitektur-Synthese
  - Automatensynthese
  - Logiksynthese
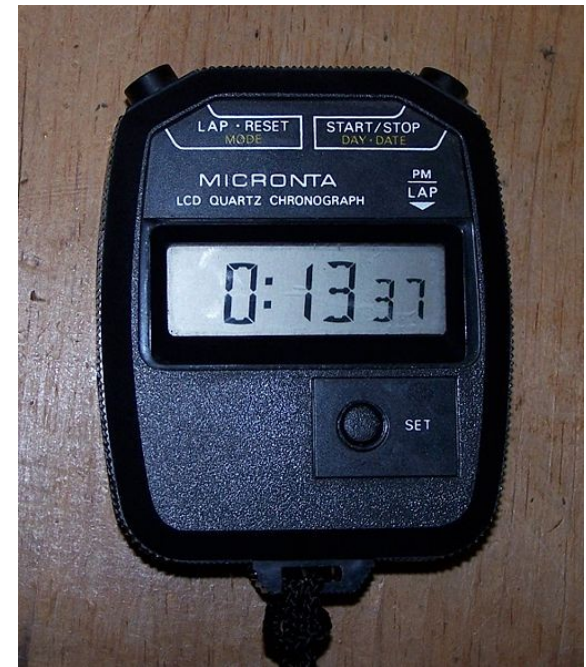 - Layoutsynthese

6 Wochen

Different specification techniques

- HDL-based specification (with and w/o templates)

- Schematics-based specification

- State diagrams

The three techniques can be combined in ISE

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Example of combining the three techniques

- Tutorials: http://www.xilinx.com/support/techsup/ tutorials/tutorials9.htm including incomplete designs.

- Text: http://www.xilinx.com/support/techsup/ tutorials/tutorials9.htm

- Complete redesign for version 9.1

- Xilinx copyright applies; not to be disclosed

© and source: http://upload.wikimedia.org/wikipedia/commons/thumb/5/54/Leet_stopwatch.JPG/510px-Leet_stopwatch.JPG

Inputs

- **strtstop**:
  Starts and stops the stopwatch. Active-low signal, acts like the start/stop button on a stopwatch.
- **reset**: Resets the stopwatch to 0:00:00.
- **clk**: External system clock for the stopwatch design.
- **mode**: Toggles between clocking and timer modes. Only functional while the clock or timer is not counting.
- **lap_load**:
  This is a dual function signal:
  In clocking mode: displays the 'Lap' display area.
  In timer mode: loads the pre assigned values from the ROM to the timer display when the timer is not counting.

Outputs

The following are output signals for the design:

- **lcd_e, lcd_rs, lcd_rw**
  Control signal for the LCD display of the Spartan-3A board
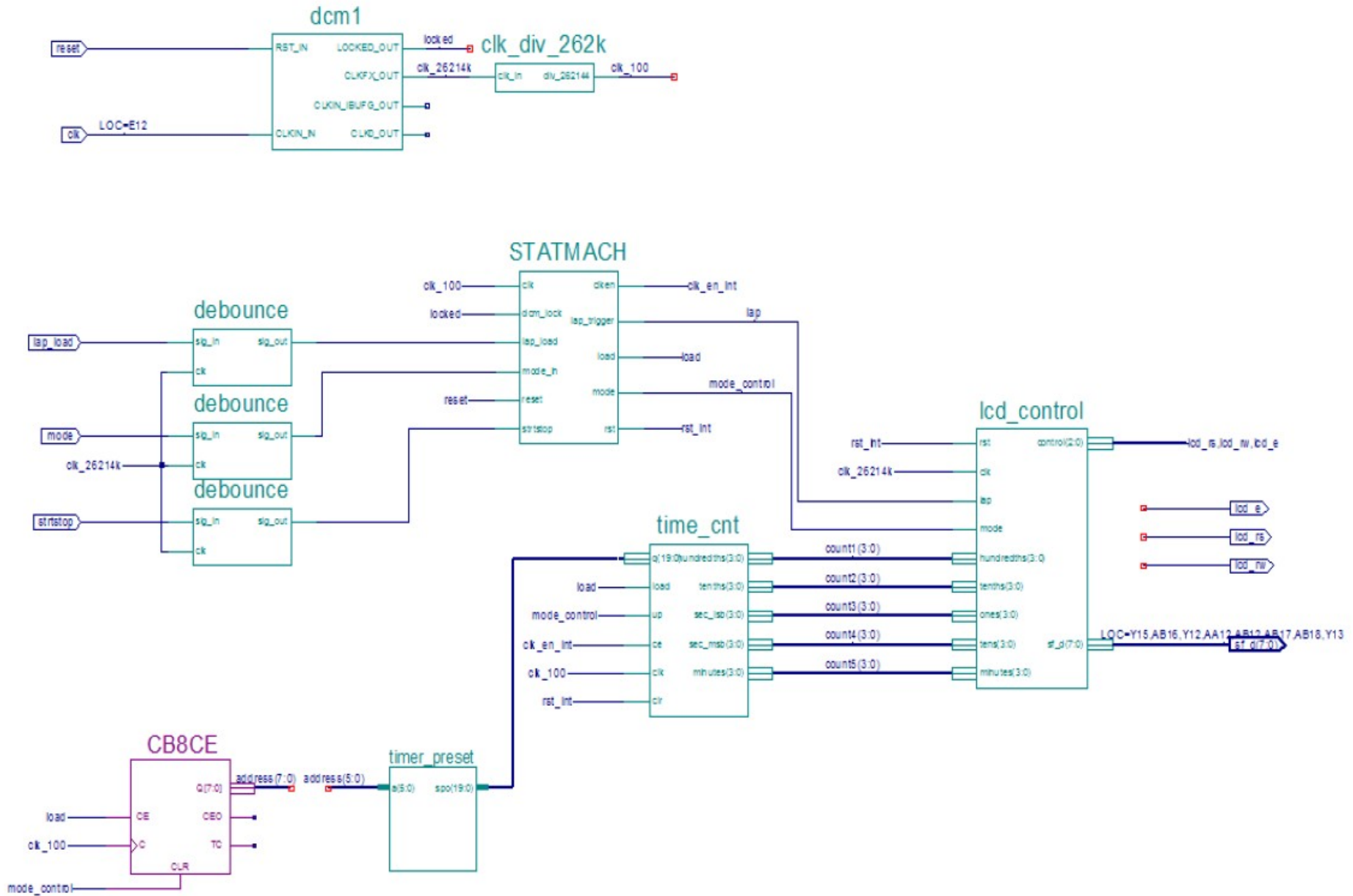
- **sf_d[7:0]**
  Data values for LCD display

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Functional blocks (1)

- **clk_div_262k:** Macro which divides a clock frequency by 262,144. Converts 26.2144 MHz clock into 100 Hz 50% duty cycle clock.

- **dcm1:** Clocking Wizard macro with internal feedback, frequency controlled output, and duty-cycle correction. The CLKFX_OUT output converts the 50 MHz clock of the Spartan-3A demo board to 26.2144 MHz.

- **debounce:** Schematic module implementing a simplistic debounce circuit for the **strtstop**, **mode**, and **lap_load** input signals.

- **lcd_control:** Module controlling the initialization of and output to the LCD display.

Functional blocks (2)

- **statmach:** State Machine module defined and implemented in State Diagram Editor. Controls the state of the stopwatch.

- **timer_preset:** CORE Generator™ 64x20 ROM. This macro contains 64 preset times from 0:00:00 to 9:59:99 which can be loaded into the timer.

- **time_cnt:** Up/down counter module which counts between 0:00:00 to 9:59:99 decimal. This macro has five 4-bit outputs, which represent the digits of the stopwatch time.

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Completed schematic

Now just follow the Xilinx tutorial

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Summary

- HDL-based specification (with and w/o templates)
- Schematics-based specification
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