

# Languages and Models of Computation (Revisted)

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# Other languages

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- **Estelle**: Designed to describe communication protocols; scope similar to SDL; unification of both failed.
- **LOTOS, Z**: Algebraic specification languages
- **Silage**: functional language for digital signal processing.
- **Rosetta**: Efforts on new system design language
- **Esterel**: reactive language; synchronous; all reactions are assumed to be in 0 time; communication based on ("instantaneous") broadcast; [//www.esterel-technologies.com](http://www.esterel-technologies.com)
- **IEC 60848, STEP 7**:  
Process control languages using graphical elements

# Levels covered by the different languages

## Requirements

## Architecture

## HW/SW

## Behavior

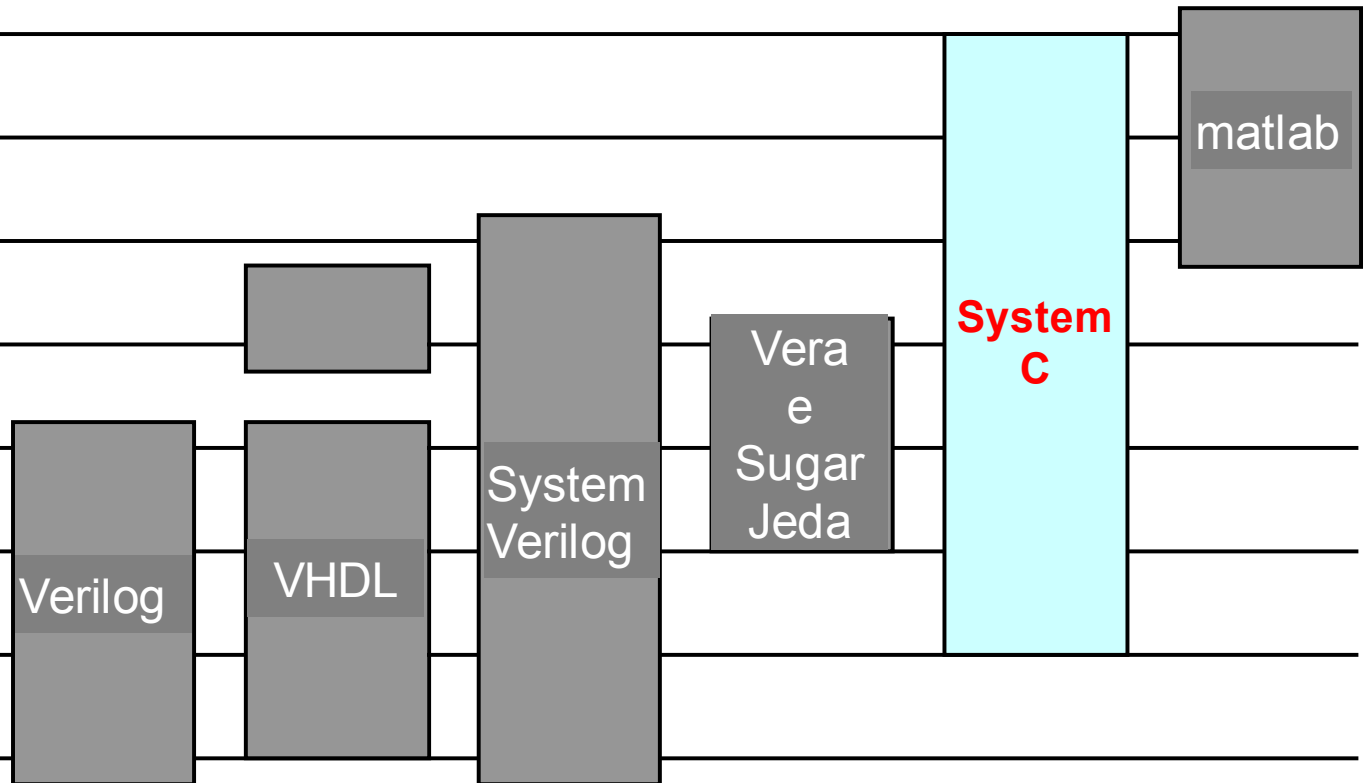
## Functional Verification

## Test bench

## RTL

## Gates

## Transistors




# Language Comparison

Language	Behavioral Hierarchy	Structural Hierarchy	Programming Language Elements	Exceptions Supported	Dynamic Process Creation
StateCharts	+	-	-	+	-
VHDL	+	+	+	-	-
SpecCharts	+	-	+	+	-
SDL	+-	+-	+-	-	+
Petri nets	-	-	-	-	+
Java	+	-	+	+	+
SpecC	+	+	+	+	+
SystemC	+	+	+	- (2.0)	- (2.0)
ADA	+	-	+	+	+

# Comparison of languages demonstrated

Communication/ local computations	Shared memory	Message passing	
		Synchronous	Asynchronous
Communicating finite state machines	StateCharts		SDL
Data flow model	Not useful		Kahn process networks
Von Neumann model	C, C++, Java	C, C++, Java with libraries CSP, ADA	
Discrete event (DE) model	VHDL, Verilog, SystemC	Only experimental systems, e.g. distributed DE in Ptolemy	

# Observations

- Useful to consider model of computation matching with the class of applications considered
- Nevertheless, feasible to simulate one model in another model (e.g. most models are simulated with imperative computing  Ptolemy)
- Commercial products available:
  - DSpace (Paderborn): Synthesis of control software for the power train in cars
  - Esterel Technologies (Toulouse): Synthesis from synchronous language SCADA (used by Airbus)



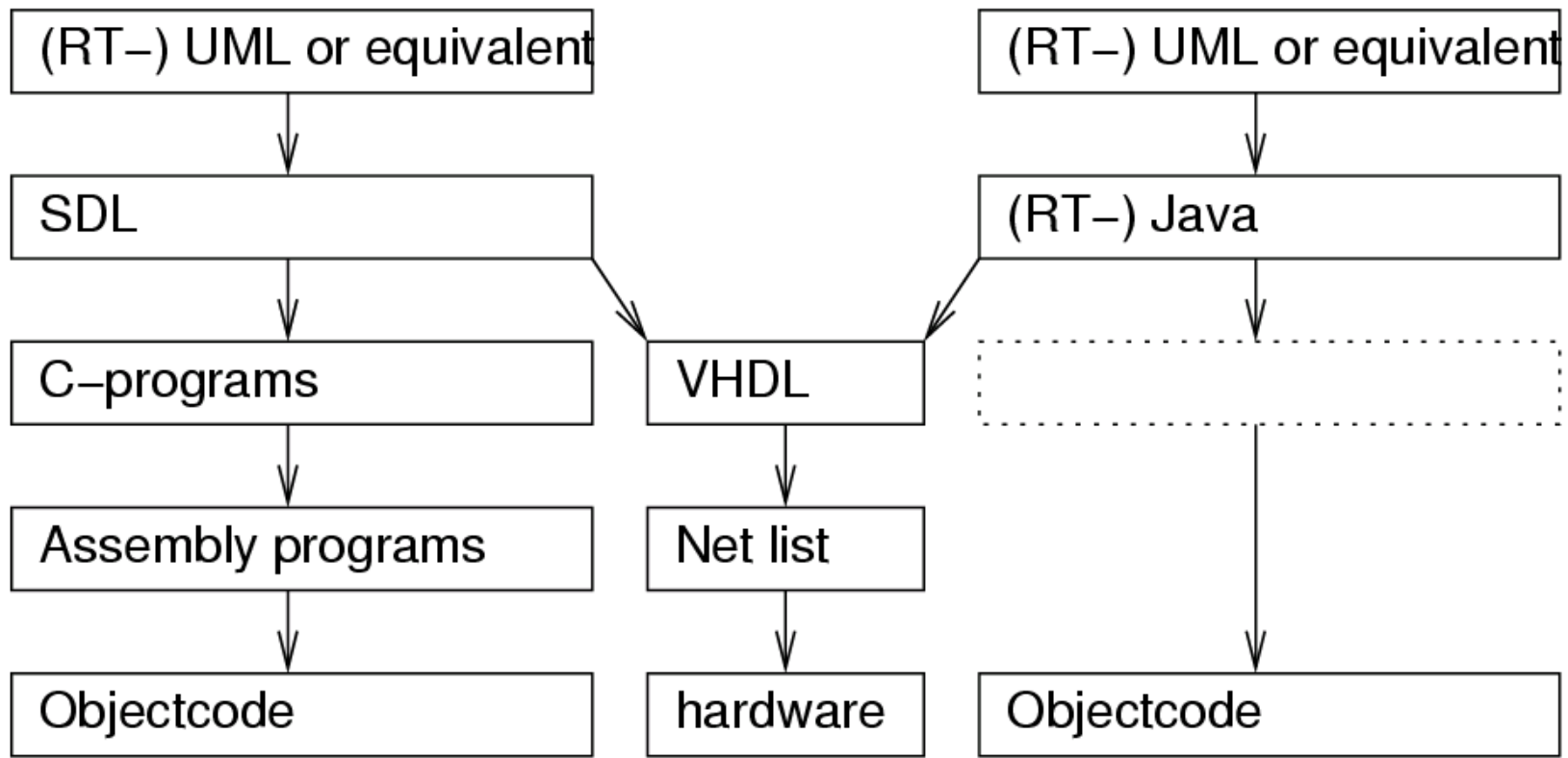
<http://www.dsace.de/w/de/gmb/home/company/dspace/pressroom/press/pr0804003.cfm>



<http://www.esterel-technologies.com/technology/success-stories/airbus.html>

# How to cope with language problems in practice?

## Mixed approaches:



# Models of computation in Ptolemy

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1. Finite state machines
2. Communicating sequential processes
3. Discrete event model
4. Distributed discrete event model
5. Process networks, including Kahn process networks
6. Synchronous dataflow (SDF)
7. Continuous time
8. Synchronous/reactive models




# UML and Model Driven Design

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# Higher levels of abstraction

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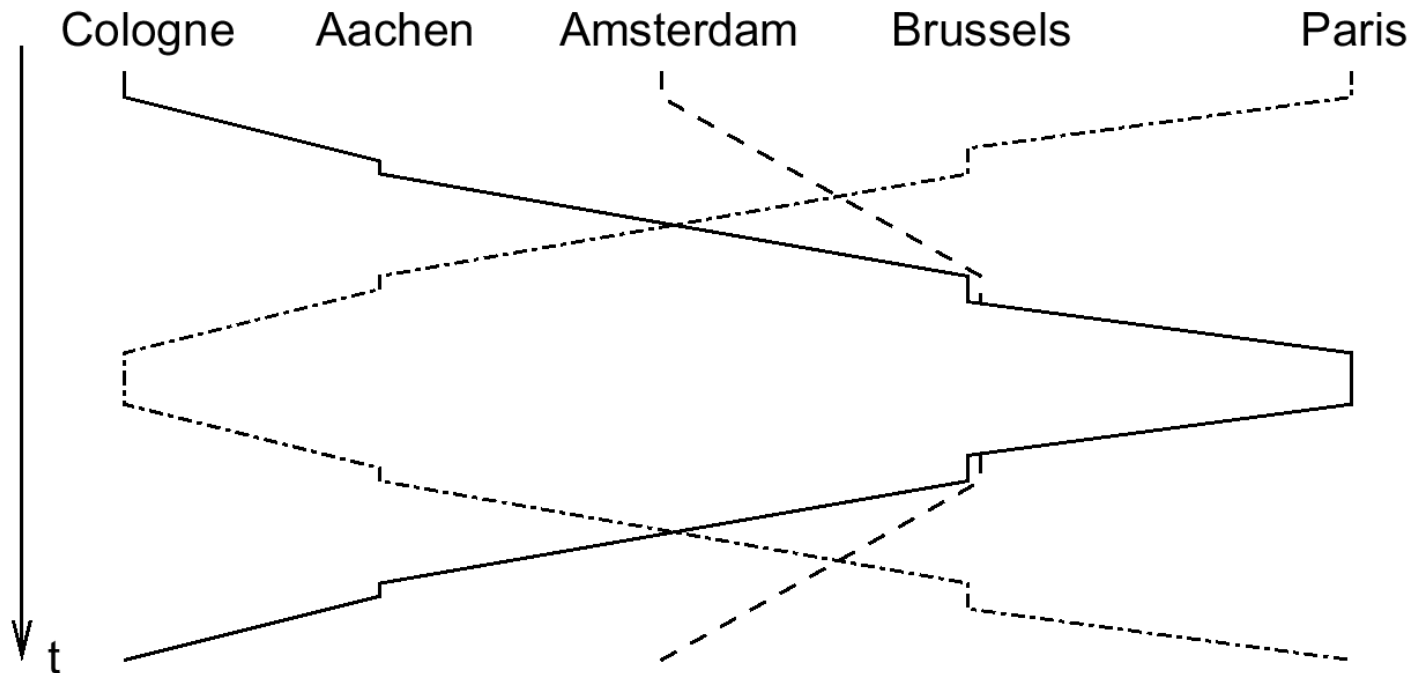
- For many applications, it is desirable to start modeling at a level higher than the (Java-, ADA-, SDL-code level)
- Special modeling mechanisms have been designed for these cases
- In particular, the unified modeling language (UML)
  - building on concepts already presented - is designed to cover this requirement  Elements



[http://portal.uni-freiburg.de/hochschulsport\\_ss2007/nuff/Hochgebirge\\_Eis.JPG](http://portal.uni-freiburg.de/hochschulsport_ss2007/nuff/Hochgebirge_Eis.JPG)

# (Message) Sequence Charts (MSC)

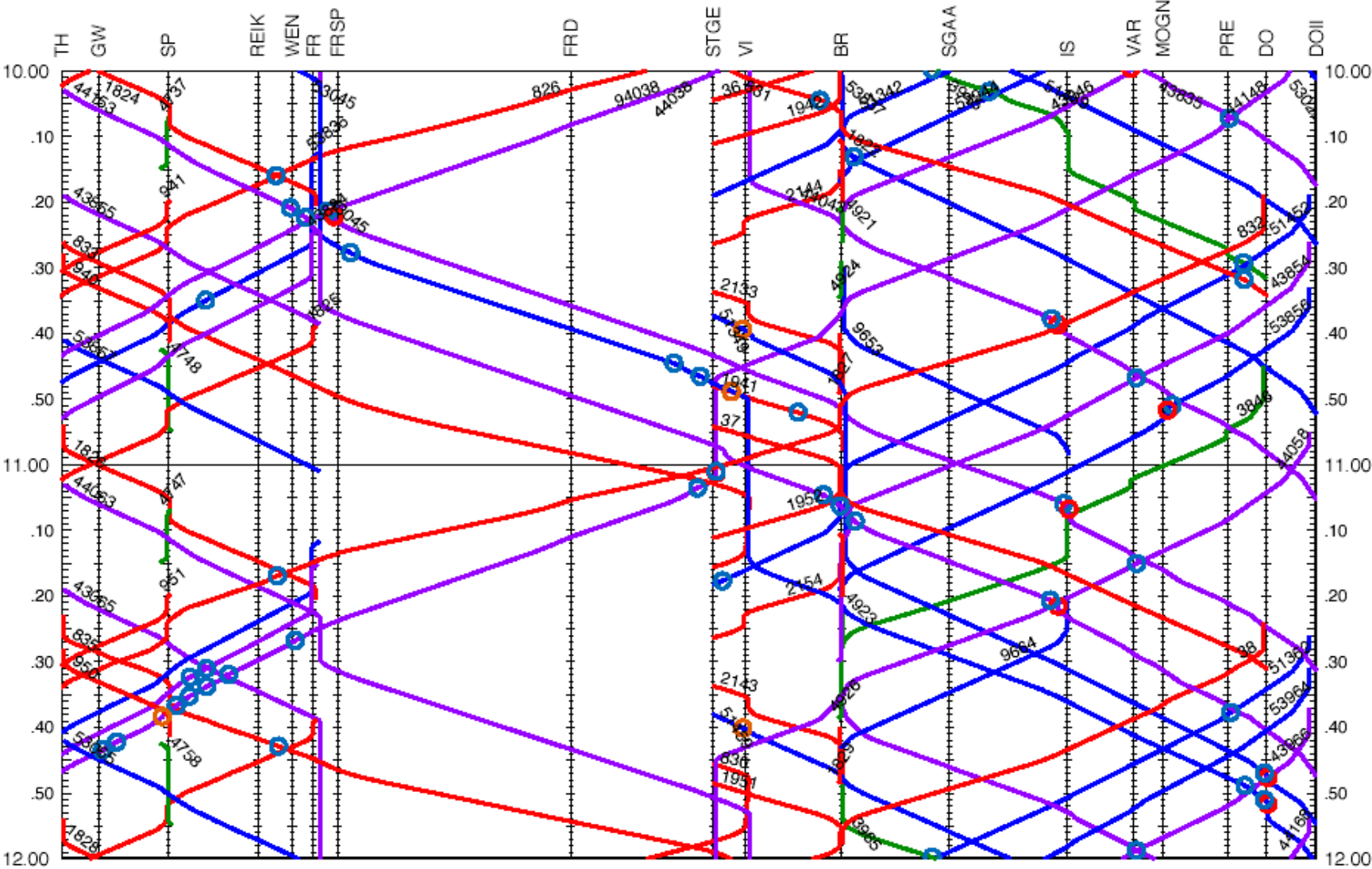
Graphical means for representing schedules; time used vertically, geographical distribution horizontally.



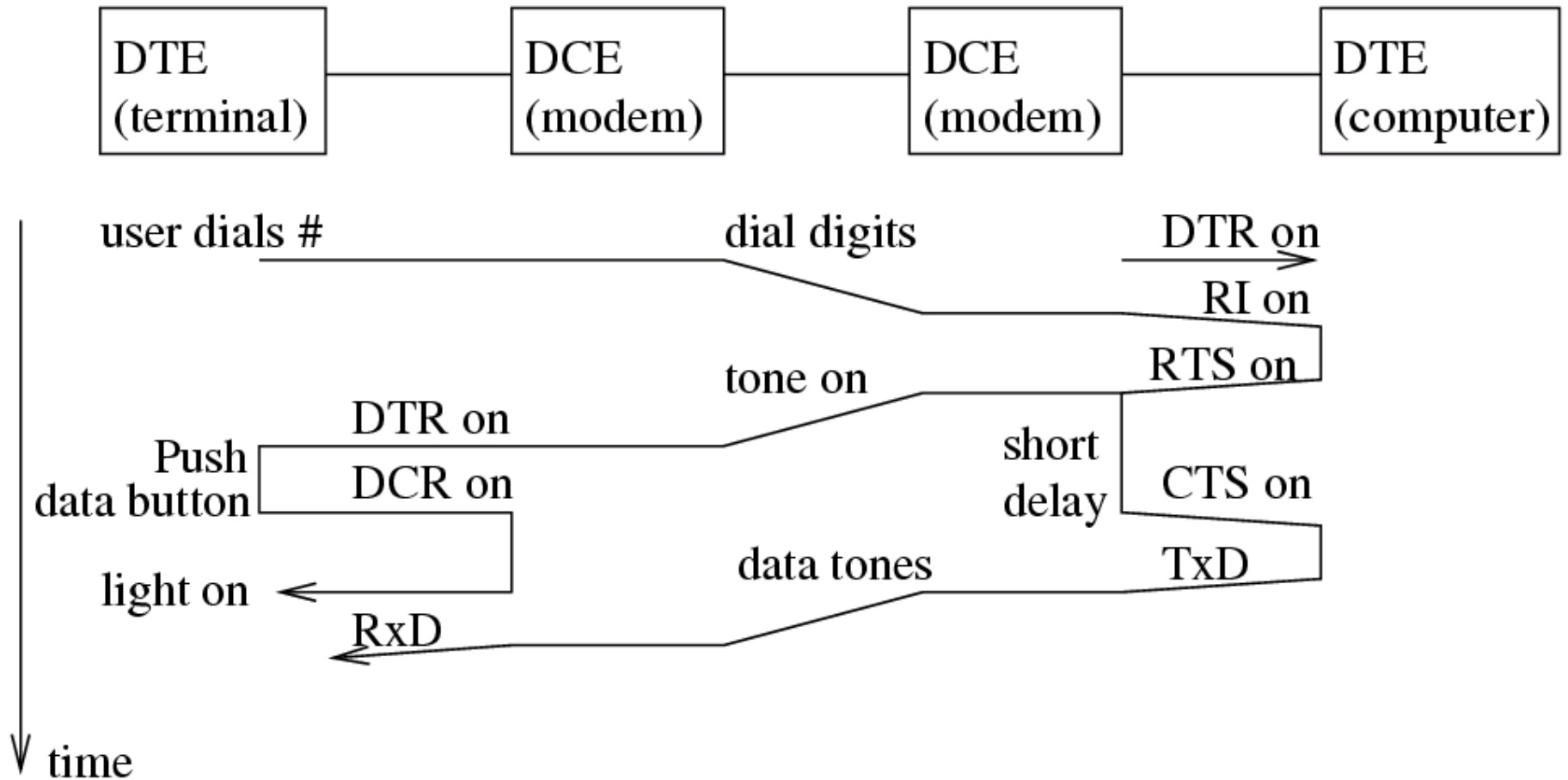
No distinction between accidental overlap and synchronization

# Time/distance diagrams as a special case

© www.opentrack.ch

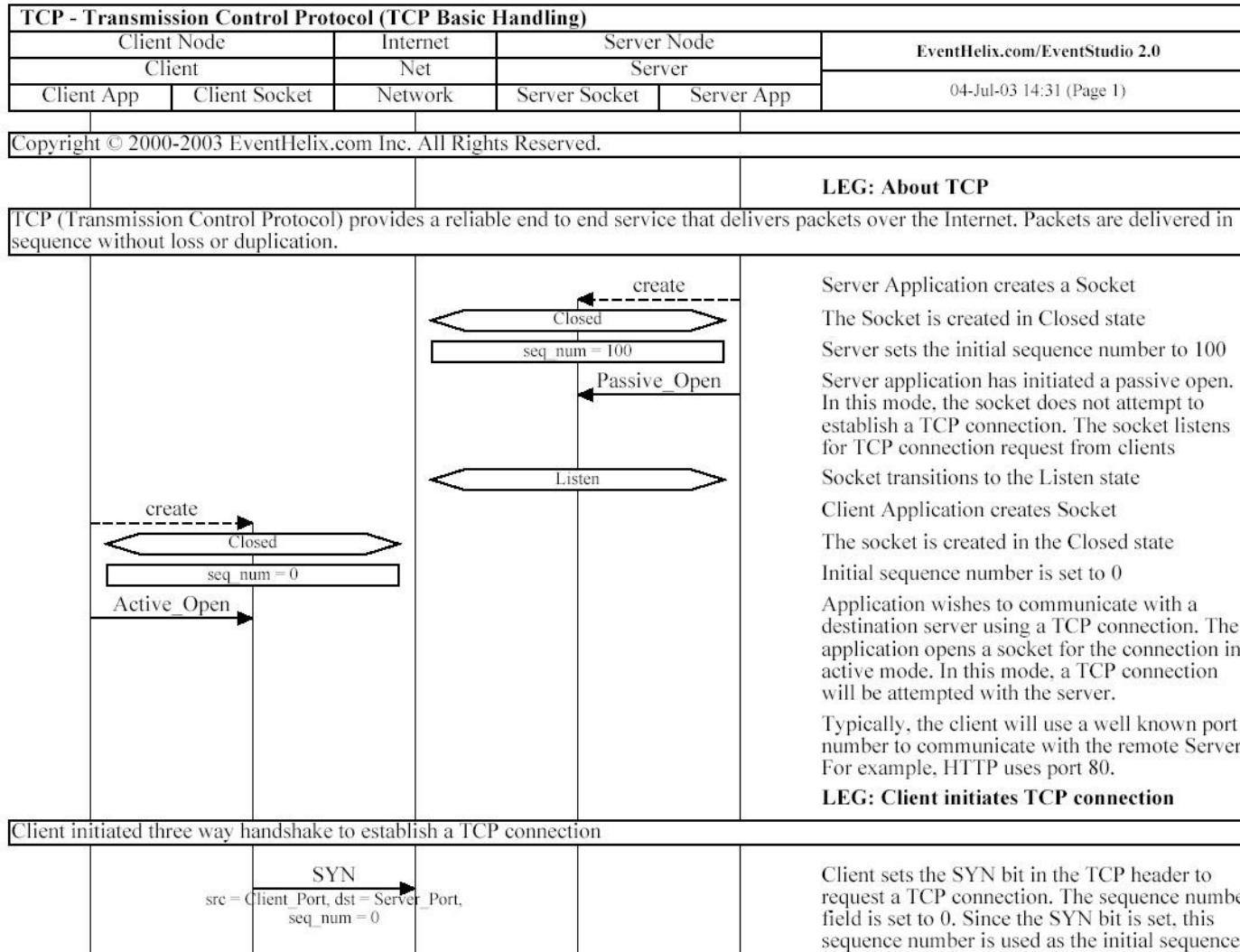


# Example 1: establishing an (old-fashioned) modem connection



According to Stallings

# Example 2: setting up a TCP connection



# (Message) Sequence Charts

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## PROs:

- Appropriate for visualizing schedules,
- Proven method for representing schedules in transportation.
- Standard defined: *ITU-TS Recommendation Z.120: Message Sequence Chart (MSC)*, ITU-TS, Geneva, 1996.
- Semantics also defined: *ITU-TS Recommendation Z.120: Message Sequence Chart (MSC)—Annex B: Algebraic Semantics of Message Sequence Charts*, ITU-TS, Geneva.

## CONS:

- describes just one case, no timing tolerances: "What *does an MSC specification mean: does it describe all behaviors of a system, or does it describe a set of sample behaviors of a system?*"  
\*

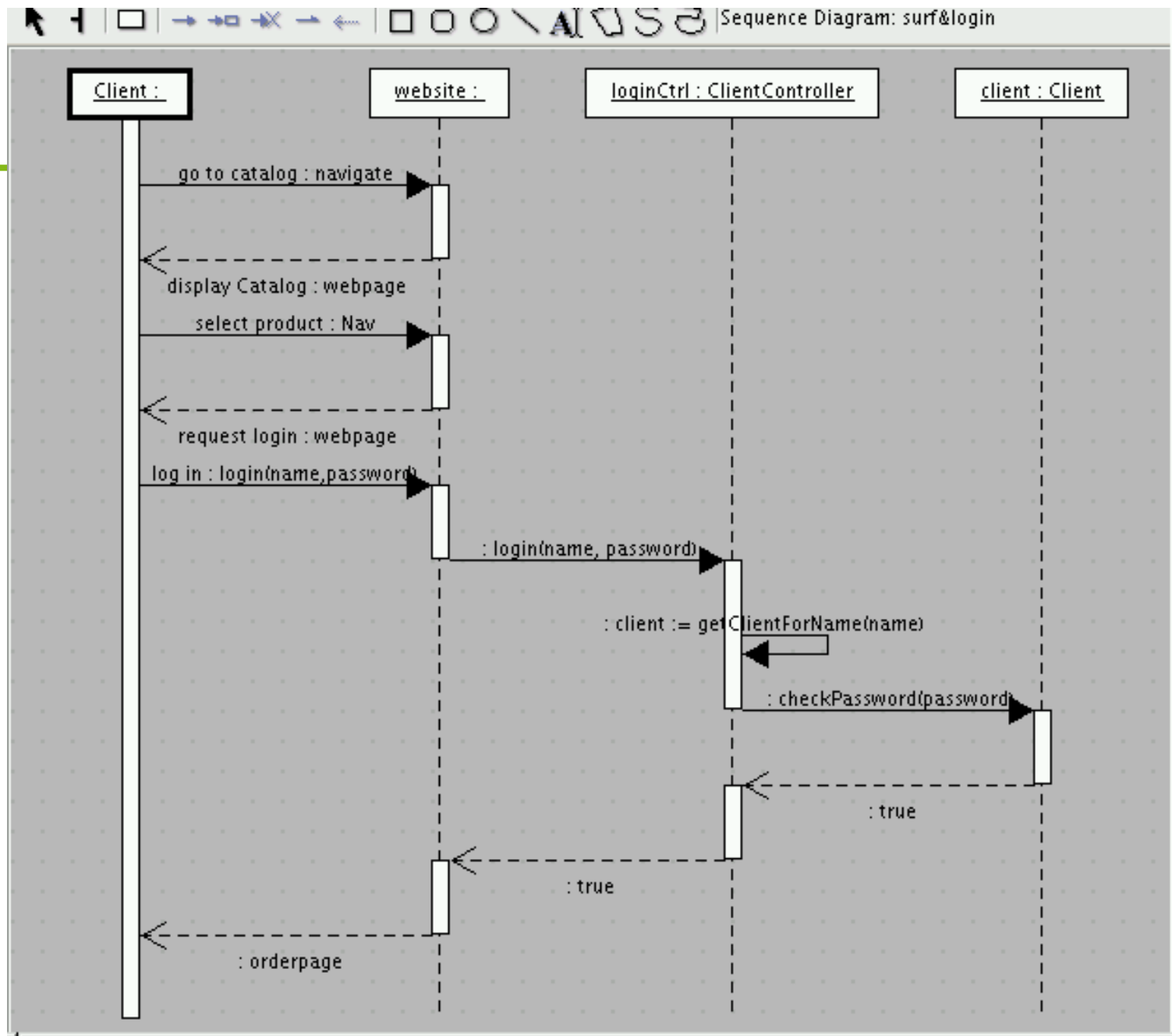
\* H. Ben-Abdallah and S. Leue, "Timing constraints in message sequence chart specifications," in *Proc. 10th International Conference on Formal Description Techniques FORTE/PSTV'97*, Chapman and Hall, 1997.

# Use in UML

Heavy usage of MSCs in UML (known as sequence diagram);

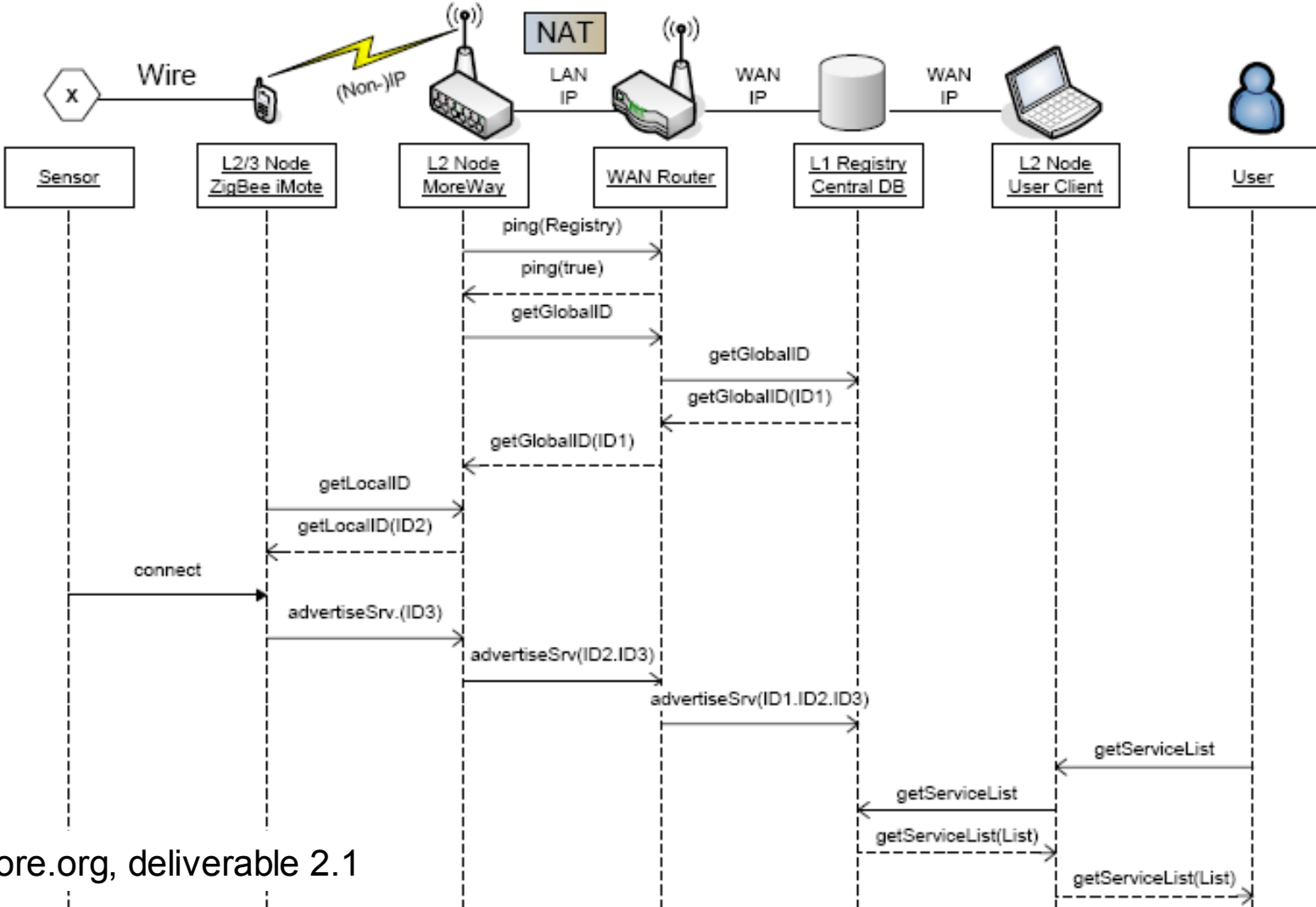
No precise timing.

Many kinds of additional elements



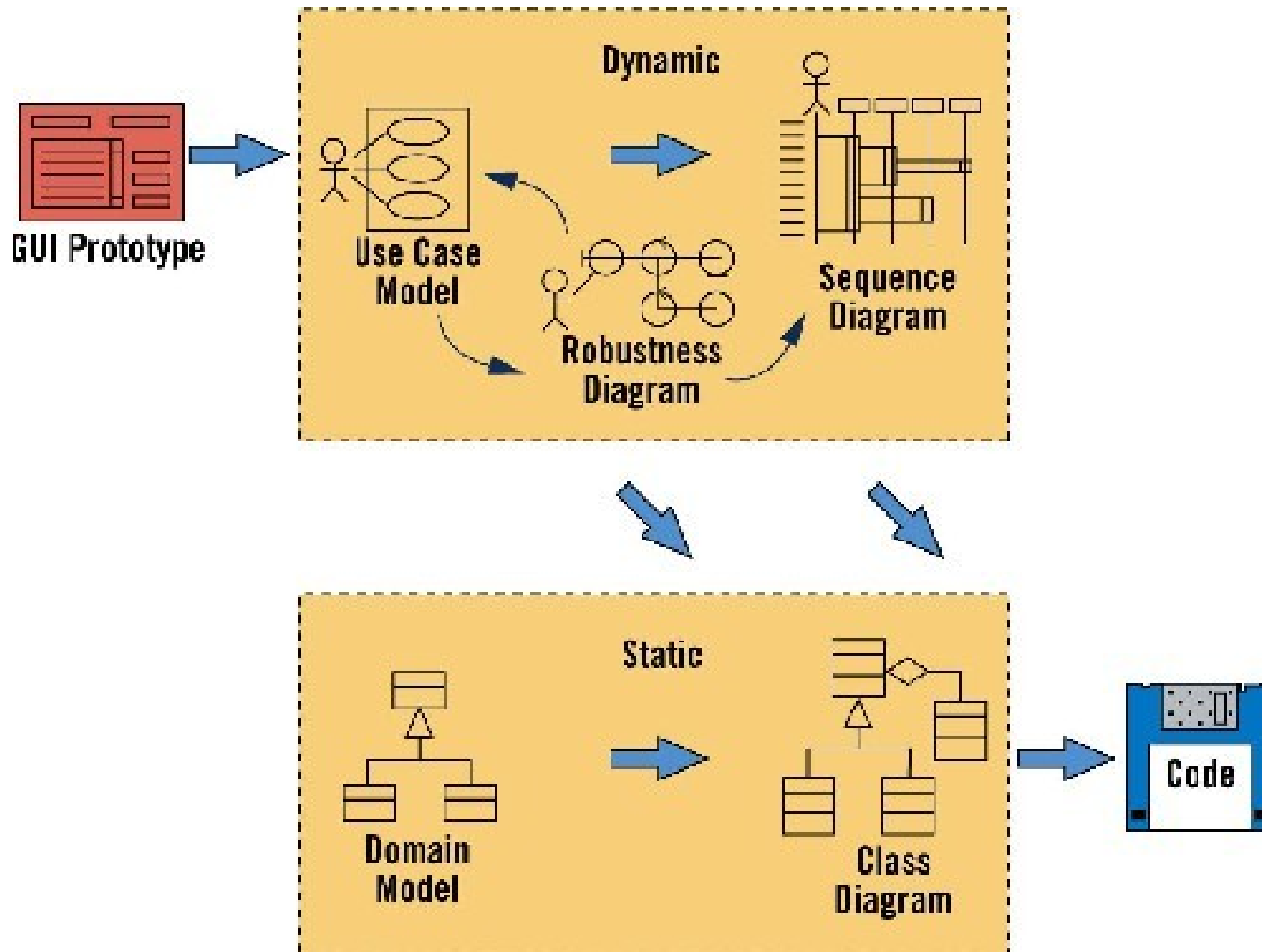


# Sequence Diagram (2)



www.ist-more.org, deliverable 2.1

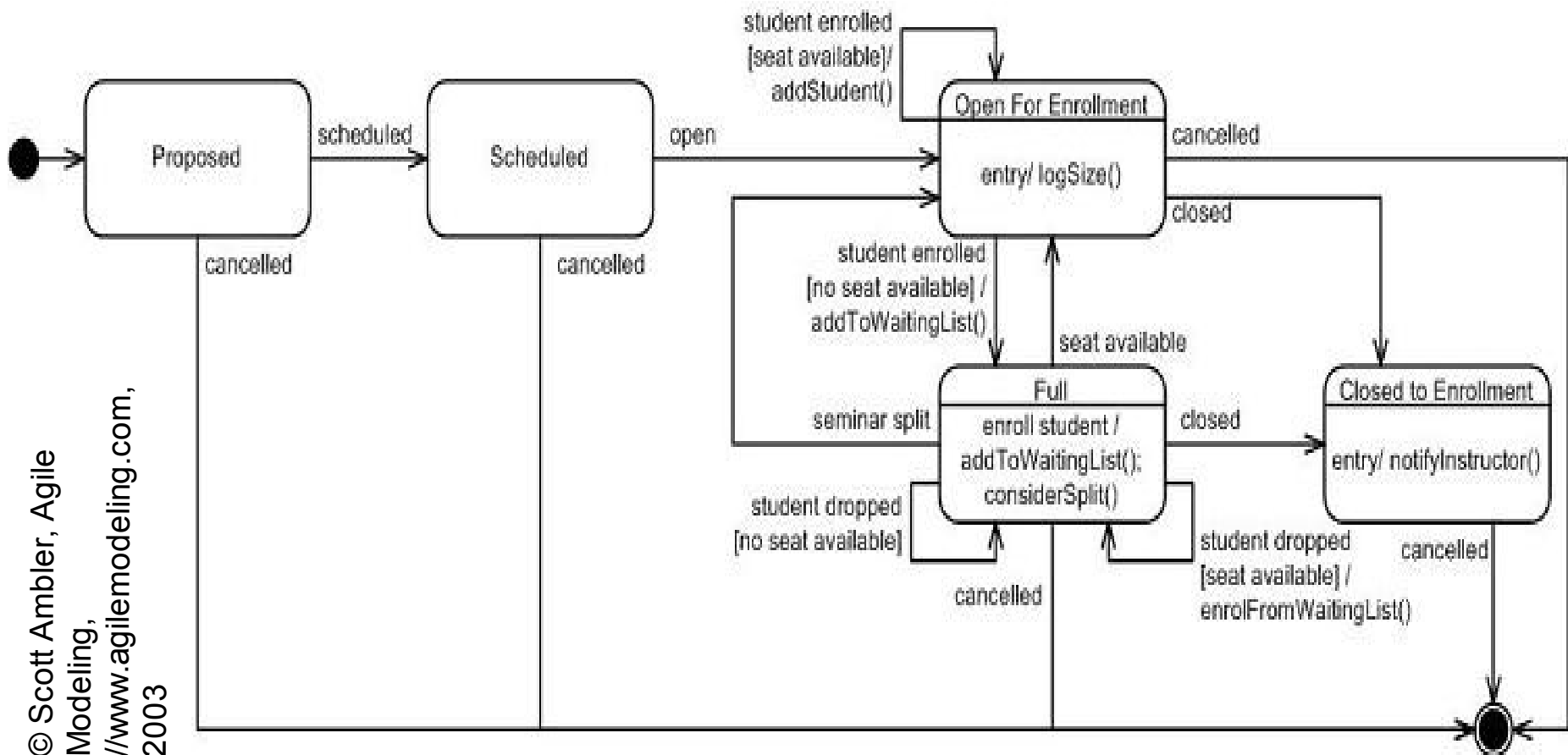
# UML diagrams



From: [www.sdmagazine.com/documents/s=815/sdm0012c/](http://www.sdmagazine.com/documents/s=815/sdm0012c/)

# State machine diagrams (UML 2.x) State diagrams (UML 1.x)

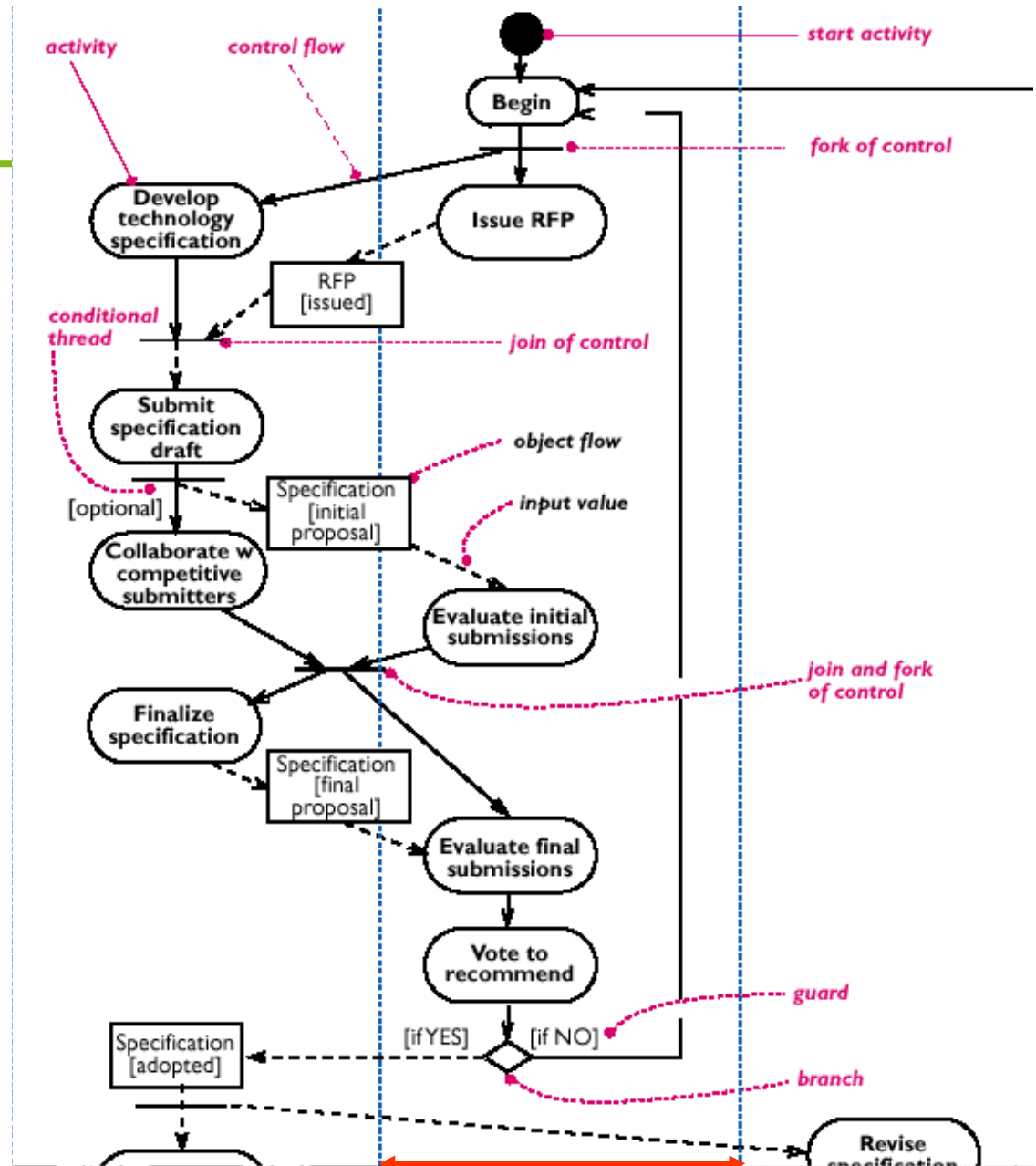
**State machine diagrams/State diagrams:**  
UML includes variant of StateCharts



© Scott Ambler, Agile  
Modeling,  
//www.agilemodeling.com,  
2003

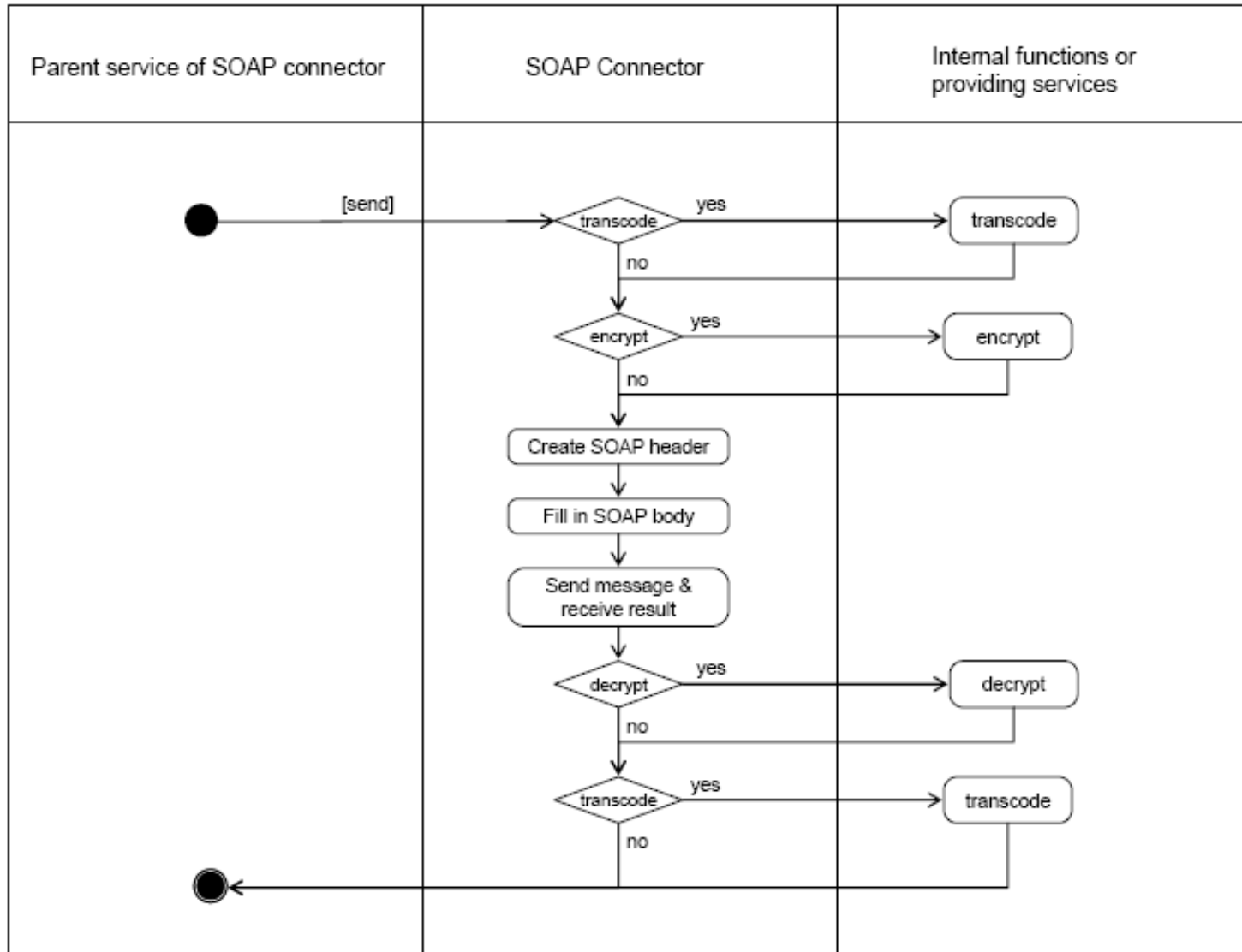
# Activity diagram

Extended Petri nets.  
Include decisions  
(like in flow charts).  
Graphical notation  
similar to SDL.

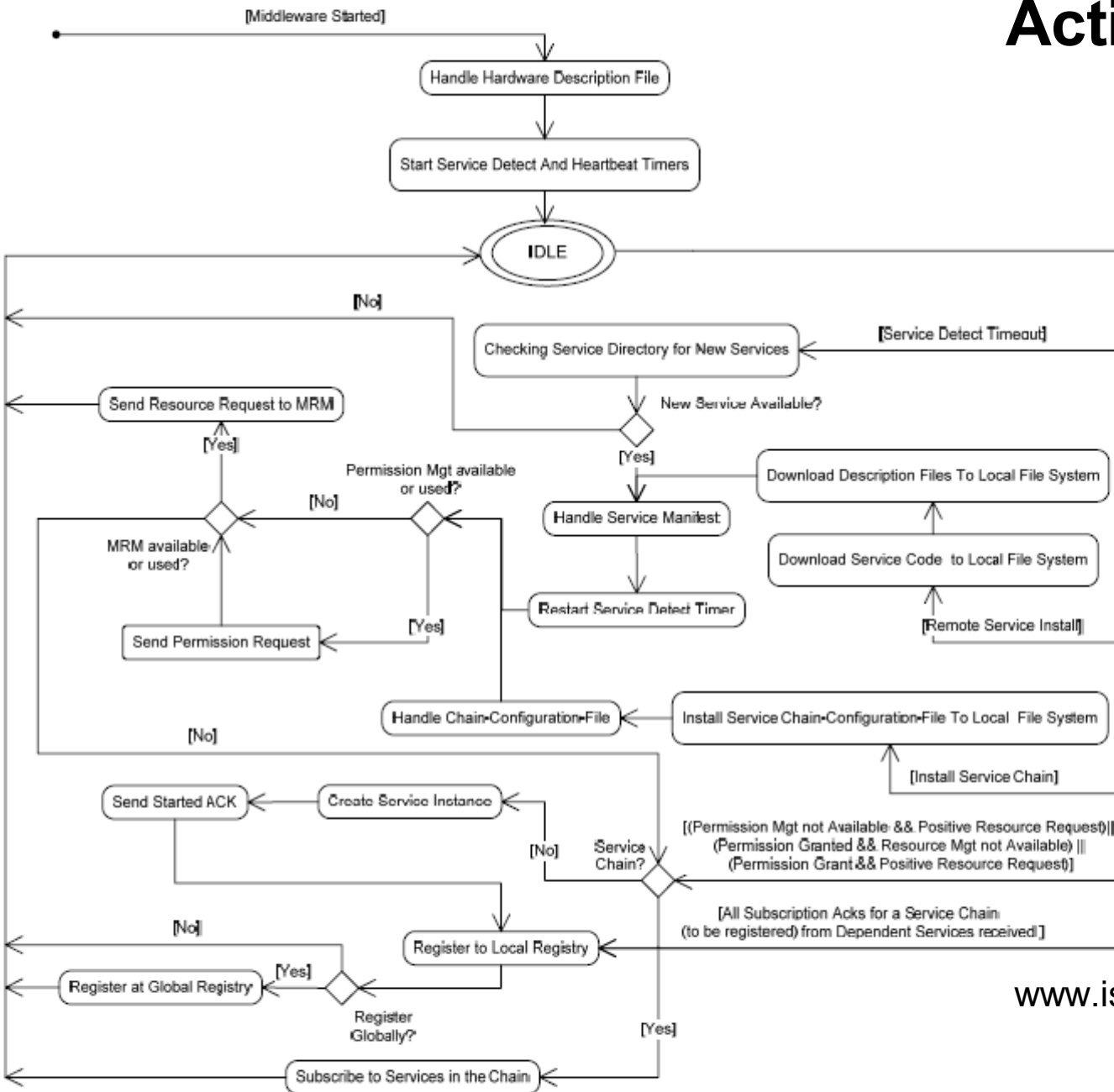


© Cris Kobryn: UML  
2001: A Standardization  
Odyssey, CACM,  
October, 1999

# Activity diagram (2)

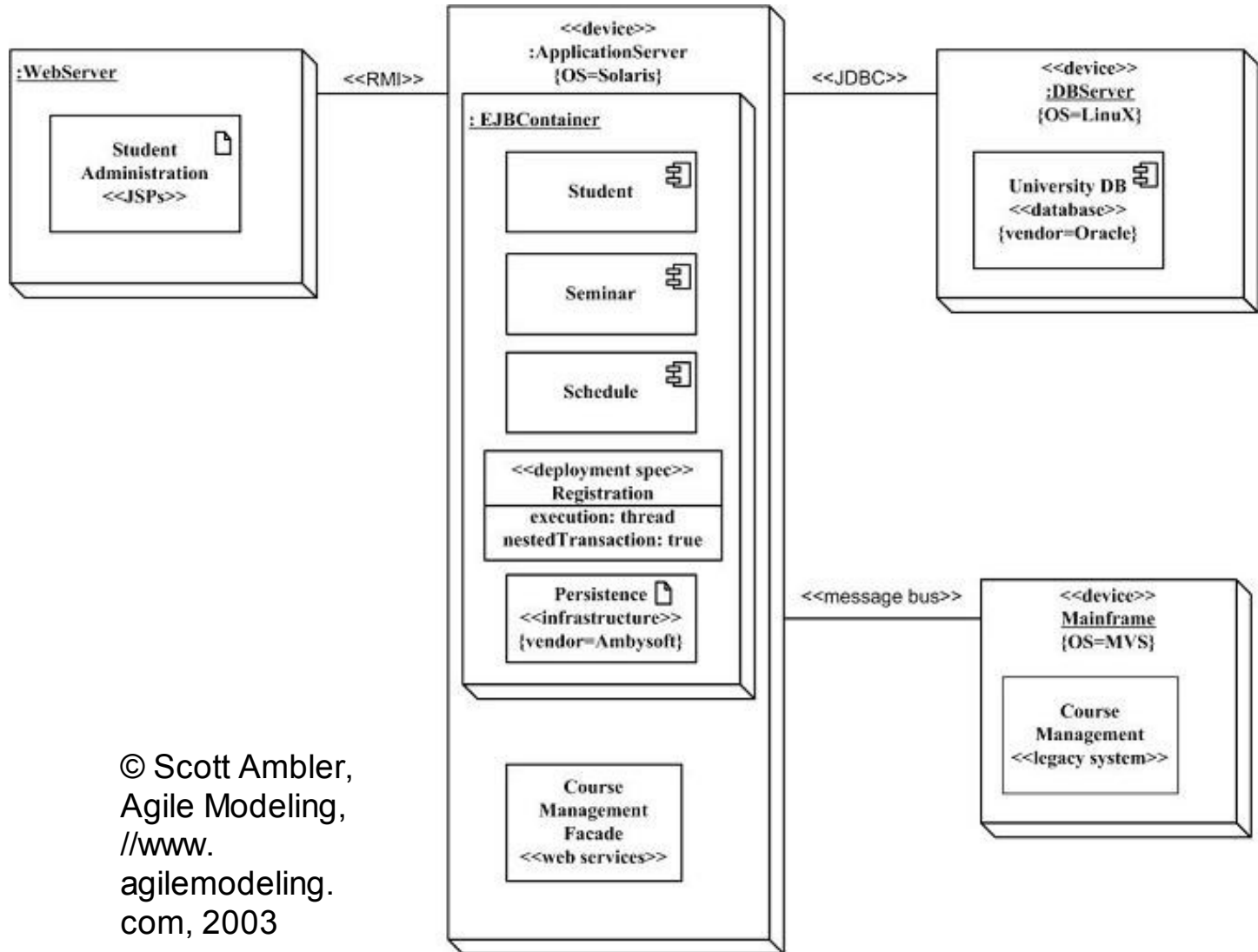


# Activity diagram (3)



# Deployment diagram

Example including some details:

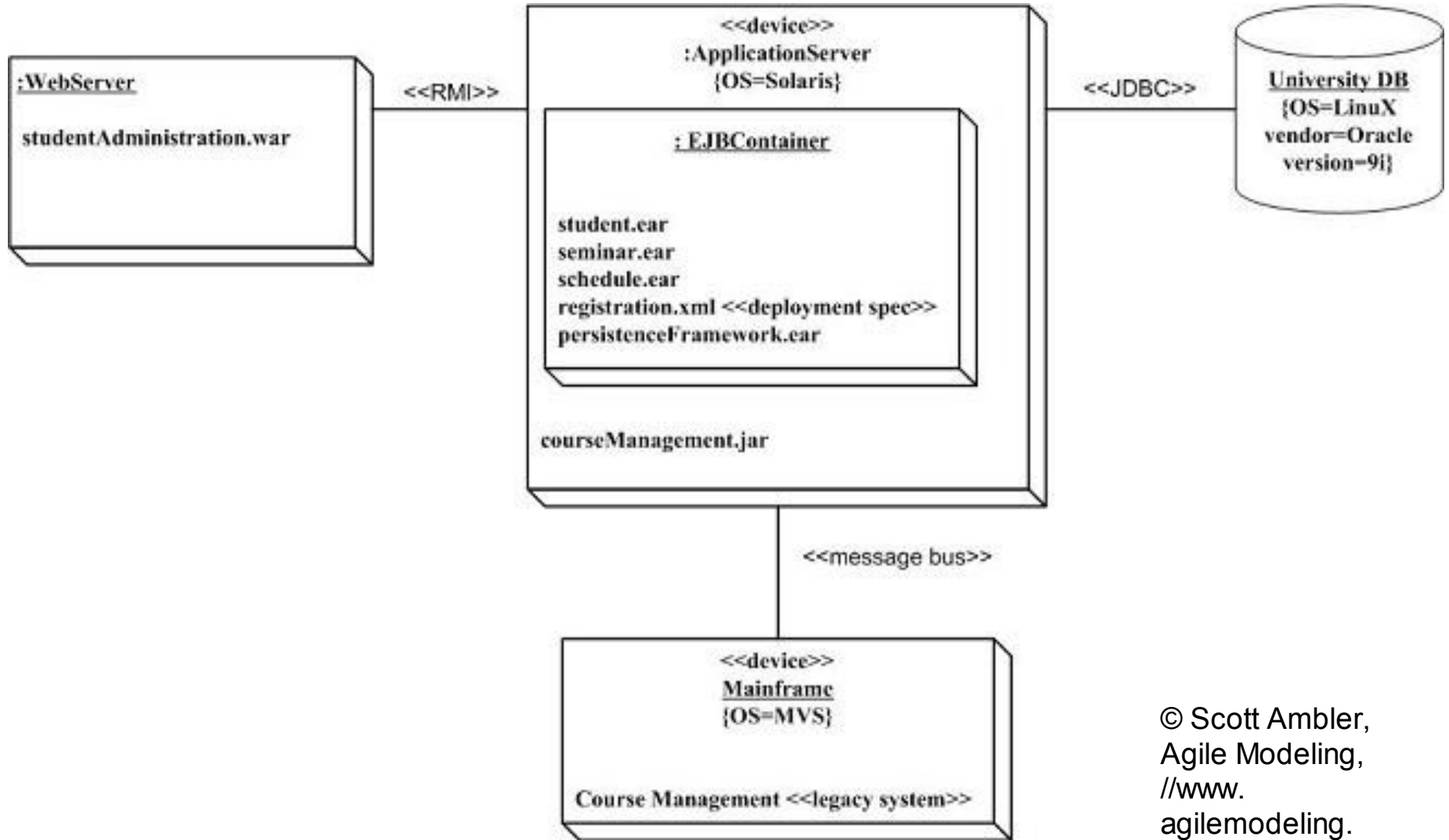


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Agile Modeling,  
[//www.agilemodeling.com](http://www.agilemodeling.com), 2003

Describe execution architecture of systems (HW or SW). Important for embedded systems.

# Deployment diagram

- More concise example -

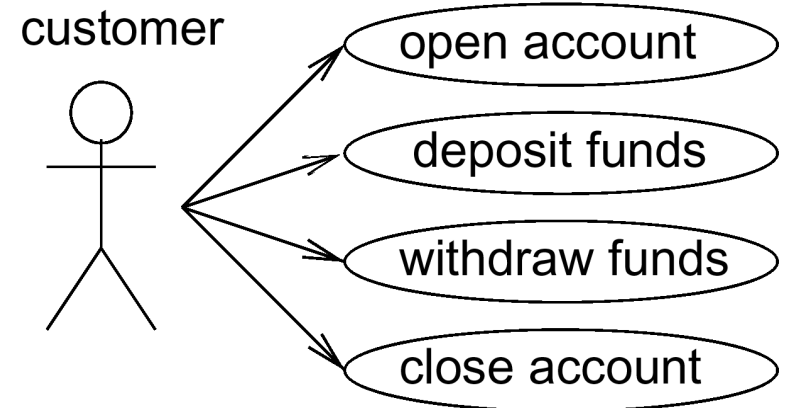
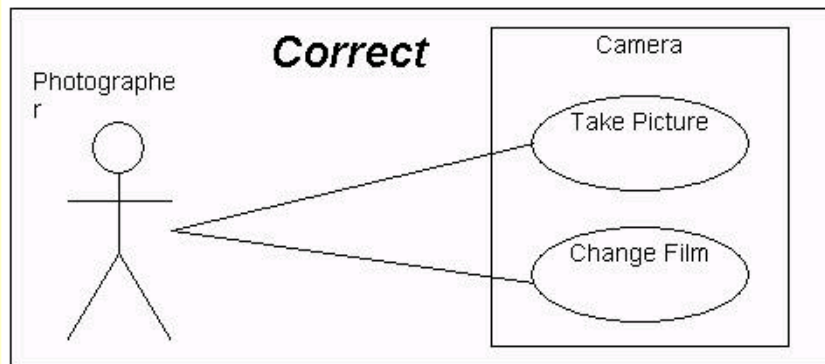


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//www.  
agilemodeling.  
com, 2003



# Use case diagram

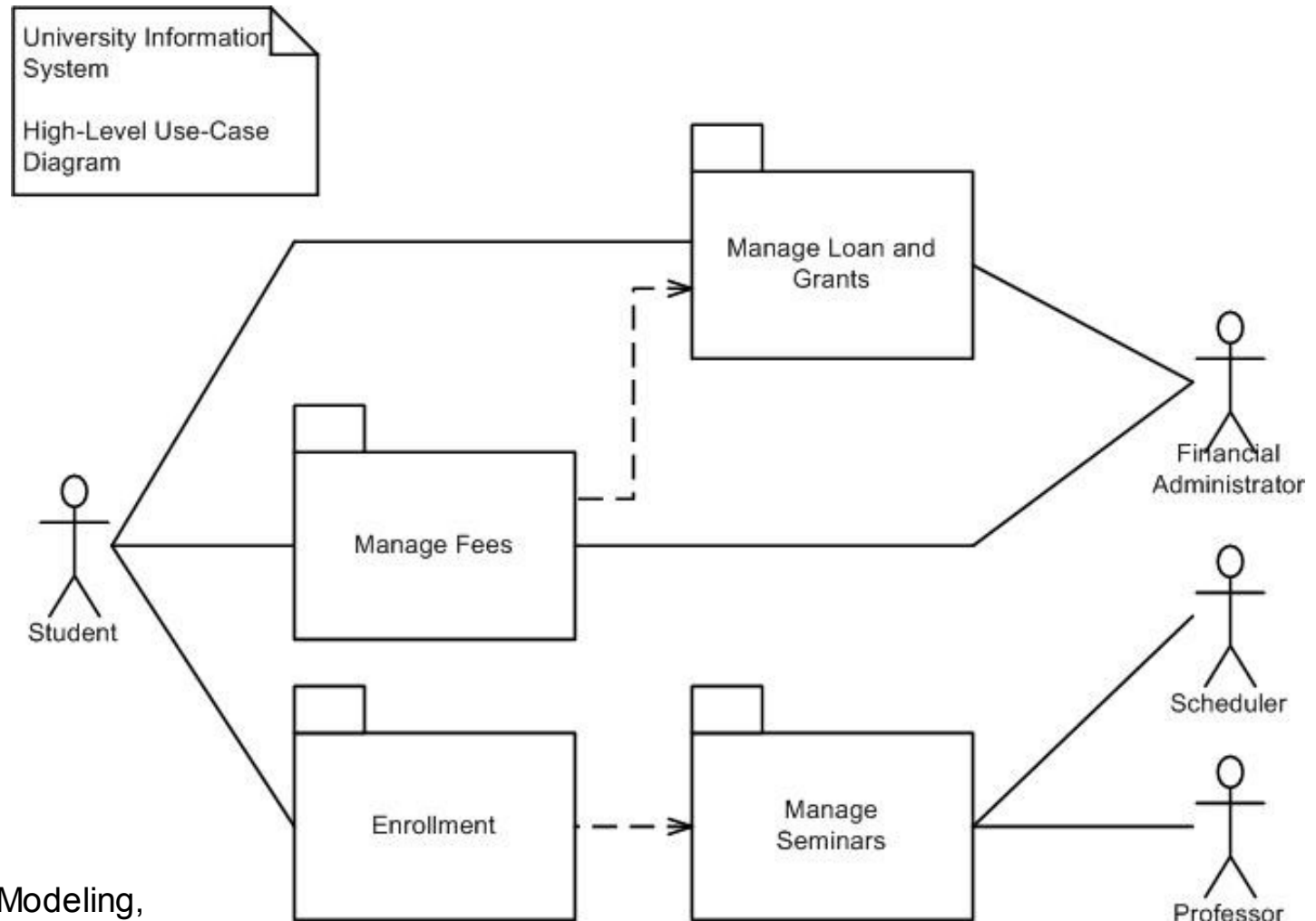
Captures typical application scenarios



# Package diagram

Represents the partitioning into packages. Introduces hierarchy.

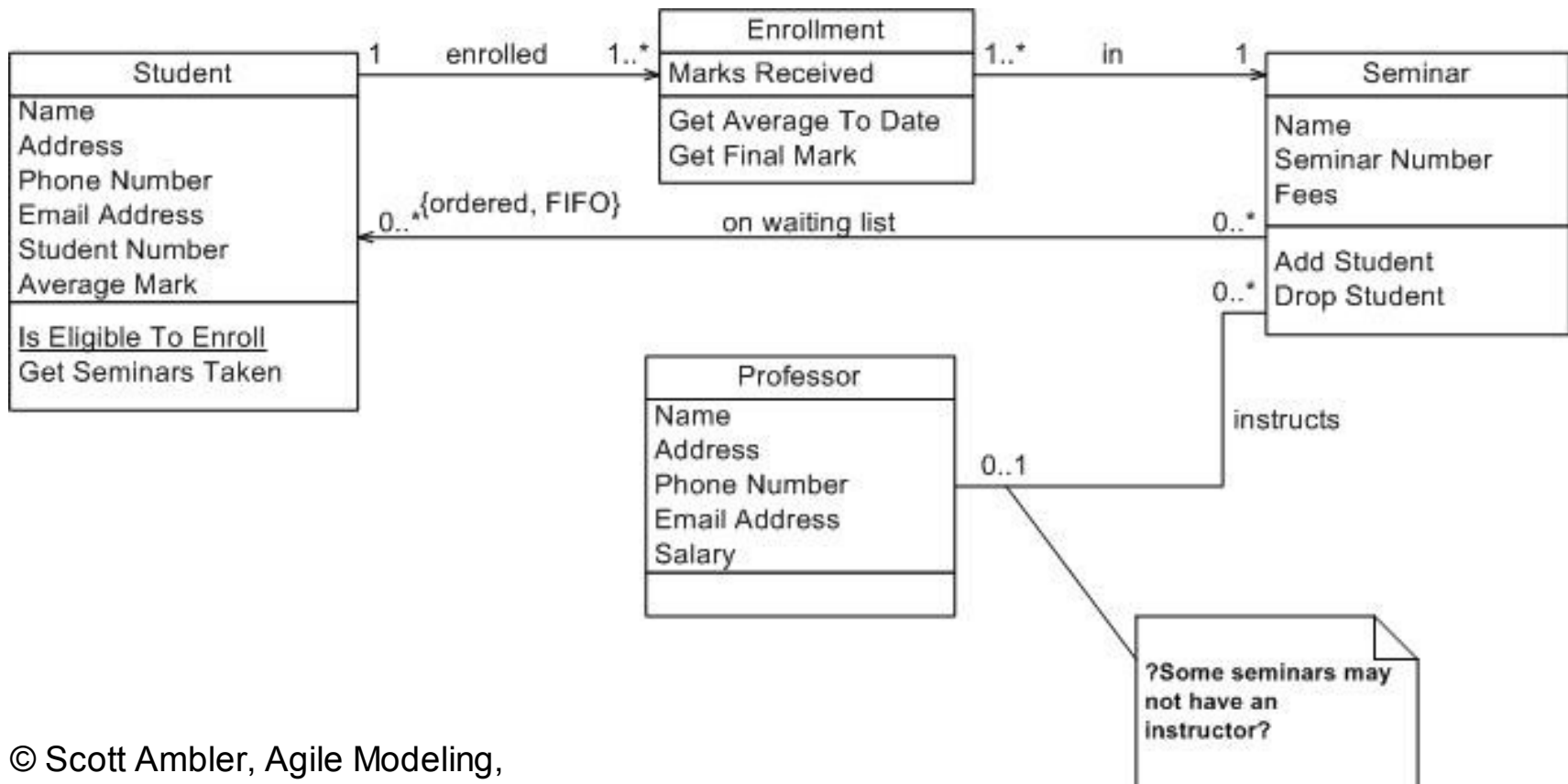
Example: Use case package diagram.



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# Class diagrams

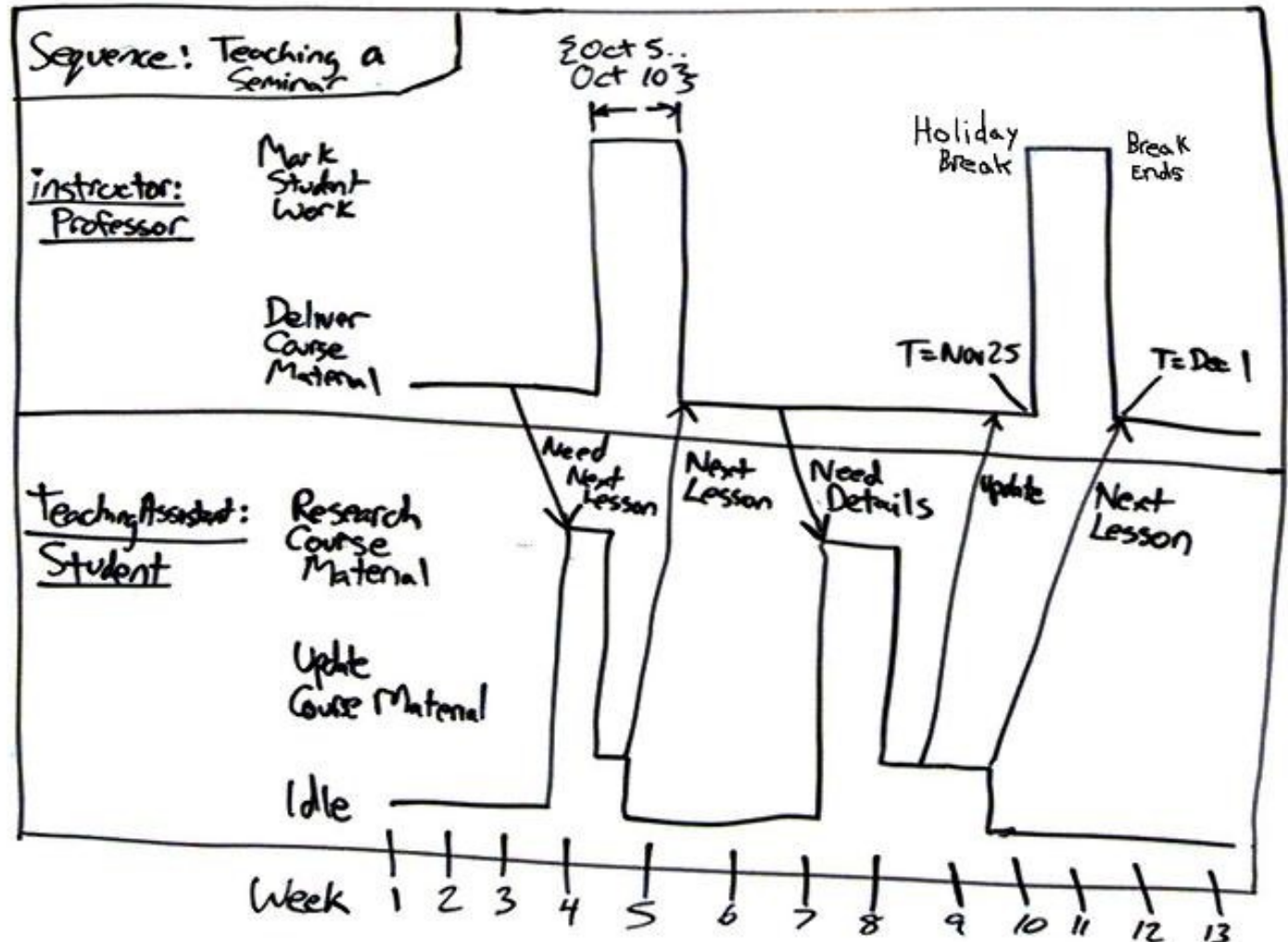
Describe object classes. Example:



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[//www.agilemodeling.com](http://www.agilemodeling.com), 2003

# Timing diagrams

Can be used to show the change of the state of an object over time.

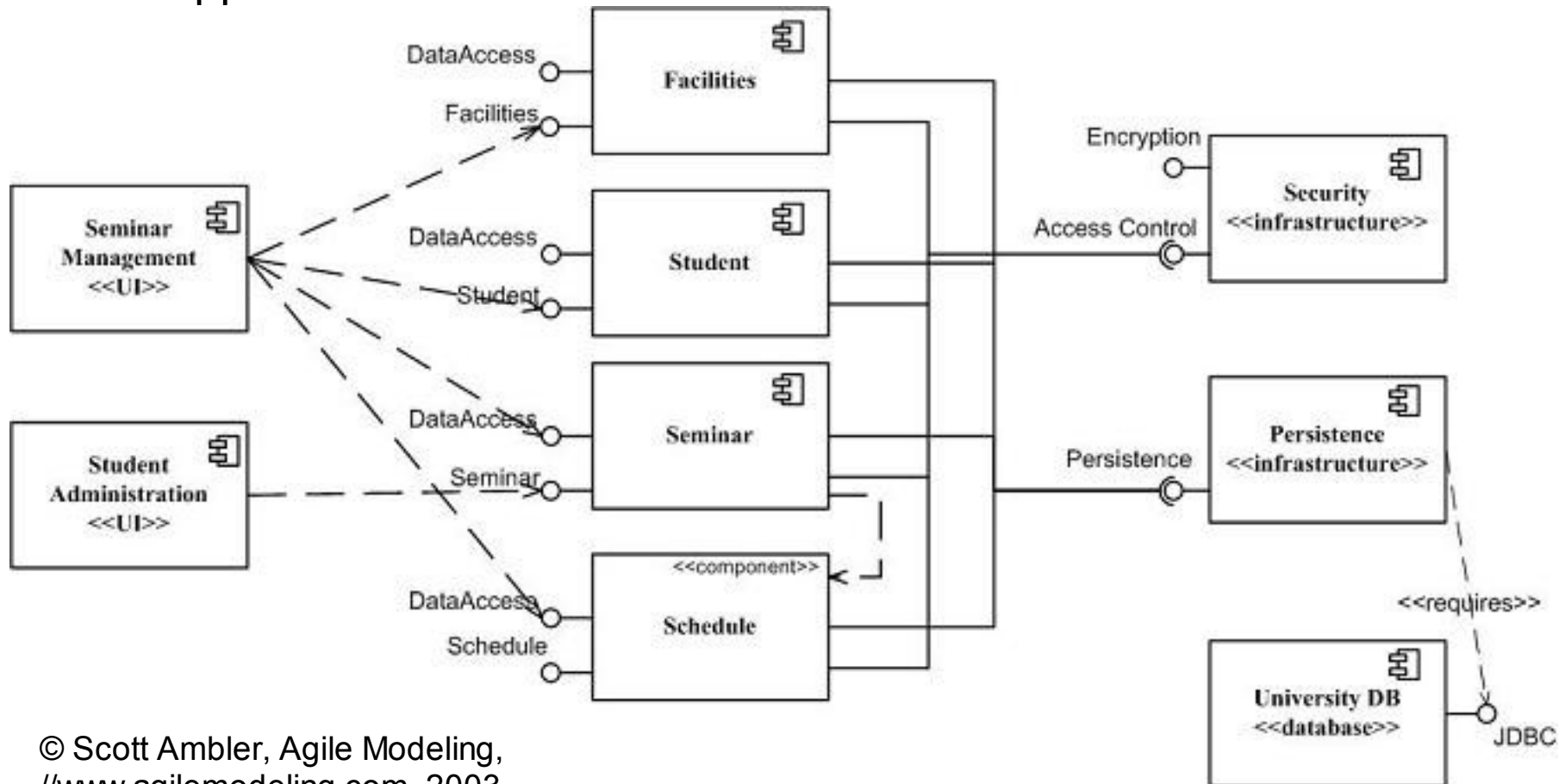


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# Component diagram

Represent components used in applications:

.. model the business software architecture, the technical software architecture, ... . Physical architecture issues, in particular hardware issues, are better addressed via UML deployment diagrams ..



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# Additional diagrams

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- **Communication diagram**  
(called collaboration diagram in UML 1.x)
  - **Object diagrams**
  - **Interaction overview diagrams**
  - **Composite structure diagrams**
- } Less frequently used

# Evaluation

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Precise specification of semantics?

Typically combined with some other “precise” language

# UML for real-time?

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Initially not designed for real-time.

Lacking features (1998):

- Partitioning of software into tasks and processes
- specifying timing
- specification of hardware components
- Projects on defining real-time UML based on previous work
- ROOM [Selic] is an object-oriented methodology for real-time systems developed originally at Bell-Northern Research.
- „UML profile for schedulability, performance and time“  
<http://www.omg.org/cgi-bin/doc?ptc/2002-03-02>



# UML Profiles Relevant for SoC

## Existing (OMG)

- SPT (Schedulability, Performance, and Timing Analysis)
- Testing Profile
- QoS and Fault Tolerance

- SysML (System Modelling Language)
- UML Profile for SoC

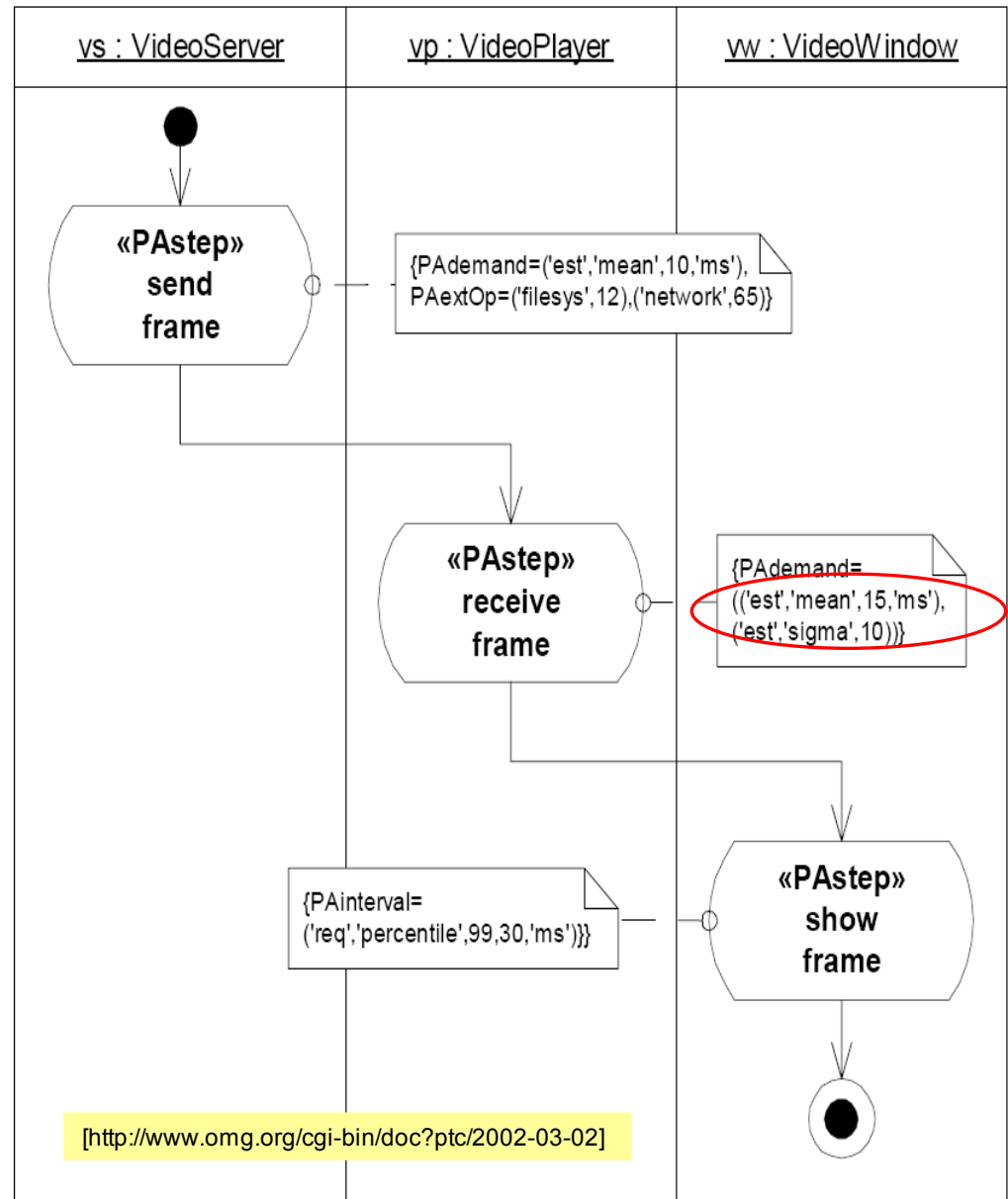
## Upcoming (OMG)

- MARTE (Modeling and Analysis of Real-Time Embedded Systems)

## non-OMG

- UML/SystemC (STMicroelectronics)
- SPRINT Profile (ST, NXP, Infineon, ...)

# Example: Activity diagram with annotations



See also W. Müller et al.: UML for SoC, <http://jerry.c-lab.de/uml-soc/>

Figure 8-10 Details of the “send video” subactivity with performance annotations

# UML Profile Summary

- **UML Profile comes as class diagrams with constraints, textual outlines (semantics), icons, diagram symbols, ...**  
Constraints and behavioral semantics typically leave several issues open (variation points)
- **Different OMG profiles of related domains may not be compatible!**
- **Current OMG UML Profiles are mainly for modelling**
- **UML Profiles do not come with a formal semantics**
- **... but Hardware Design is not just modelling**
- **HW verification and synthesis requires a well-defined and precise behavioral semantics**
- **Several UML tools already support UML profile definition**

# Summary

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- Message sequence charts
  - Original (ITU) version, Time-Distance diagrams
  - Sequence diagram in UML
- UML
  - State machine diagram (StateChart-like)
  - Activity diagram (extended Petri nets)
  - Deployment diagram (exec. arch.),
  - Use case diagram
  - Package diagram (hierarchy), Class diagrams,
  - Timing diagrams (UML 2.0), UML for real-time?