

# Assignment 4

(10 Points)

**Deadline is Tuesday, June 1, 2010, 12:00**

**Note:** Make use of an arbitrary VHDL development environment like *Symphony EDA* or *GHDL/GtkWave* to model and verify your components. This is also useful to draw waveforms if required. *If submitted by e-mail, please provide a single PDF or PS file only.*

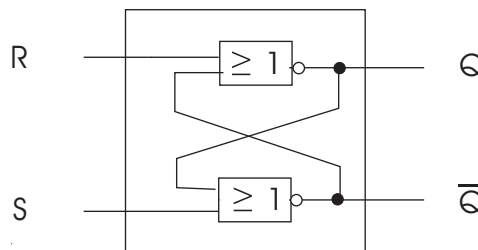
## 4.1 VHDL Syntax (5 Points)

In the lecture, a full-adder written in VHDL has been presented. Extend this initial example to form an N-bit ripple carry adder. Such an adder passes the carry-bit from one “stage” to the next, therefore the term *ripple carry*.

1. Draw the general structure of an N-bit ripple carry adder. To do this, exploit the regularity of the full-adder component.
2. Specify the structural description for a 4-bit *RCA* in VHDL. Make use of the basic code presented in the lecture.

## 4.2 Timing semantics in VHDL simulations (5 Points)

1. Explain the term *delta-cycle* concisely and give an example of how/where it is used.
2. An RS latch is a bistable memory element composed of two NOR-gates with mutual feedback as shown below:



Describe this element’s behavior in VHDL. Suppose that each NOR-gate gives rise to a delay of *1ns*. Declare all signals to be of type *Bit*. Draw the waveforms, given this component is stimulated as follows:

S <= '0' after 0 ns, '1' after 5 ns, '0' after 10 ns  
 R <= '0' after 0 ns, '1' after 15 ns, '0' after 20 ns

Regarding the initialization of signals, is there any special care to be taken? Also, explain concisely whether or not (and why) *delta-cycles* are required for simulation.

**General notes:**

Dates and additional information can be found at <http://ls12-www.cs.tu-dortmund.de/en/teaching/courses/ss10/ies/>. The assignments will usually be published **Tuesdays** on a weekly basis and have to be solved until the next **Monday**. Drop your sheets into the mailbox in OH16 right across the secretariat (E22) or send an e-mail to your tutor. In the latter case, the submissions must be of either **PDF** or **PS** format. To pass the labs a minimum of 60% of the total points must be achieved.