jan.kleinsorge [☺] tu-dortmund.de
michael.engel [☺] tu-dortmund.de

Exercises to
Introduction to Embedded Systems
Summer term 2010

Assignment 8

(10 Points)

Deadline is Wednesday, June 30, 2010, 12:00

8.1 D/A conversion (5 Points)

Consider the following D/A converter:

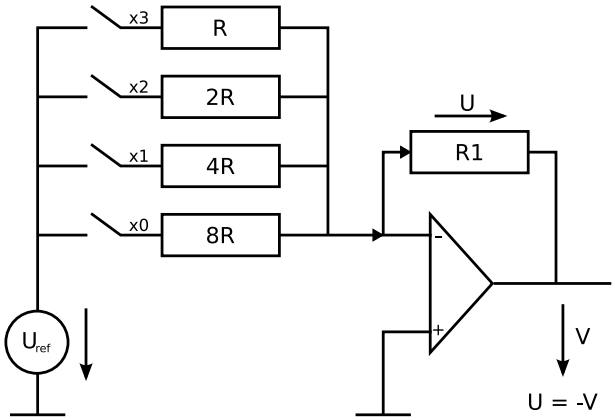

Figure 1: DAC

Given $U_{ref} = 5V$, $R = 1k\Omega$:

- Specify the effective resistance value of $R1$, given that the digital values shall be mapped onto a voltage range of $0 - 10V$?
- The precision of the D/A conversion is highly dependend of the precision (tolerance) of the resistors employed. Given a sufficiently large deviation from the desired value, the monotonicity does not hold, so that a current resulting from a digital value b is lower than the value resultung from the next lower digital value $b - 1$.
  - Between which binary values b and $b - 1$ will such an error in resistance have the greatest impact?
  - Calculate the resulting currents for these values, respectively.
  - How large (in Ω) may the maximum deviation (upwards) become, so that no error in monotonicity occurs?

Hint: For further explanations see the online preview of the book "Embedded Systems" (`http://ls12-www.cs.tu-dortmund.de/de/teaching/courses/ws0910/es/book/`*)*

(Turn around . . .)

8.2 Shared resources (5 Points)

Given the following task set for a single CPU with a_i denoting the activation times and c_i the execution durations, respectively. In addition, $\Delta_p(S_r)$ denotes in which cycle relatively to a_i a task requests access to a shared resource S_r. Inversely, $\Delta_V(S_r)$ denotes after how many execution cycles the resource is released.

	a_i	c_i	$\Delta_P(S_1)$	$\Delta_V(S_1)$	$\Delta_P(S_2)$	$\Delta_V(S_2)$
T_1	{3,10}	4	1	4	-	-
T_2	{0,17}	3	-	-	1	2
T_3	{12}	6	-	-	4	6
T_4	{7}	7	2	5	-	-

The static priorities are assigned such that $T_1 > T_2 > T_3 > T_4$, with unrestricted preemption otherwise.

1. Consider a resource access management *without priority inheritance*. Draw a diagram which depicts the task executions. Mark the intervals in which priority inversion occurs and point out which tasks are being blocked by others, respectively.

2. In contrast to such an unrestricted blocking behavior, how would the schedule look like given the *priority inheritance protocol* is applied. Give a **concise** explaination of the changes in execution.

General notes:

Dates and additional information can be found at `http://ls12-www.cs.tu-dortmund.de/en/teaching/courses/ss10/ies/`. The assignments will be published **Tuesdays** on a weekly basis and have to be solved until the next **Monday**. Drop your sheets into the mailbox in OH16 right across the secretariat (E22) or send an e-email to your tutor. In the latter case, the submissions must be of either **PDF** or **PS** format. To pass the labs a minimum of 60% of the total points must be achieved.