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Exercises to
Cyber-physical System Fundamentals
Summer term 2012

Assignment 4

(10 Points)

Deadline is Tuesday, May 29, 2012, 12:00

Note: It is a good idea to make use of some VHDL development environment like *VHDL Simili* (Symphony EDA) or *GHDL/GtKWave* (a template for the latter can be found on EWS or the course homepage) to model and verify your components. This is also useful to draw waveforms, if required.

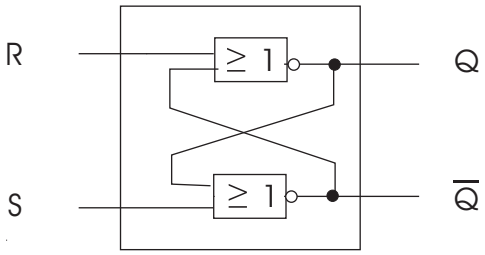
4.1 VHDL Syntax (5 Points)

In the lecture, a full-adder written in VHDL has been sketched (slides 2.06/40ff provide additional material). Extend this initial example to form an N-bit ripple carry adder (RCA). Such an adder passes the carry-bit bit from one "stage" to the next, therefore the term *ripple carry*.

1. Draw the general structure of an N-bit ripple carry adder. To do this, exploit the regularity of the full-adder component.
2. Specify the structural description for a 4-bit *RCA* in VHDL. Make use of the basic code presented in the lecture.

4.2 Timing semantics in VHDL simulations (5 Points)

1. Explain the term *delta-cycle* consicely and give an example of how/where it is used.
2. An RS nor latch is a bistable memory element composed of two NOR-gates with mutual feedback as shown below:



Describe this element's behavior in VHDL. Suppose that each NOR-gate gives rise to a delay of *1ns*. Declare all signals to be of type *Bit*. Draw the waveforms, given this component is stimulated as follows:

S <= '0' after 0 ns, '1' after 5 ns, '0' after 10 ns
R <= '0' after 0 ns, '1' after 15 ns, '0' after 20 ns

Regarding the initialization of signals, is there any special care to be taken? Also, explain concisely whether or not (and why) *delta-cycles* are required for simulation.

General notes:

Dates and additional information can be found on the lecture website (via EWS). The assignments will be published **Tuesdays** on a weekly basis and have to be solved until the next **Monday** unless stated otherwise. Drop your sheets into the mailbox in OH16 right across the secretariat (E22) or send an e-email to your tutor. In the latter case, the submissions must be of either **PDF** or **PS** format. To pass the labs, a minimum of 50% of the total points must be achieved.