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Exercises to
Cyber-physical System Fundamentals
Summer term 2012

Assignment 7

(10 Points)

Deadline is Monday, June 18, 2012, 12:00

7.1 A/D-Conversion (5 Points)

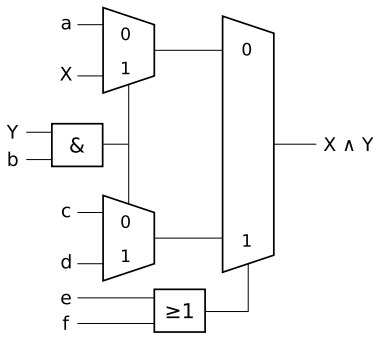
To convert an analog signal into its digital approximation, the conversion technique of *successive approximation* has been presented in the lecture. Convert the following analog inputs into their corresponding digital values using this technique: $U_{in} = 2.25V, 3.75V$ and $1.8V$. Specifiy for each input and for each step of the approximation cycles:

- the reference voltage U_{ref}
- the intermediate binary representation

The digital representation shall consist of a 4 bit wide bit vector. The range of values shall be assumed to be $[U_{min}, U_{max}] = [1.0V, 4.75V] = [0000_2, 1111_2]$

7.2 FPGA structure (2 Points)

Given the following structure of a CLB block in an FPGA circuitry:



- For the given multiplexer-based CLB, specify appropriate input values so that the block realizes the boolean function $x \wedge y$.
- Independently from this CLB, specify how the functions $x \vee y$ and $\neg x$ can be realized with a single multiplexer.

7.3 CPU-Technologies (3 Points)

For the construction of embedded systems the use of (instruction) processors is predominant. In the lecture, different types of processors have been presented, namely *ASIC*, *DSP* and *VLIW*. Briefly list their characteristics regarding field of application, requirements and special characteristics of the instruction set and the memories.

General notes:

Dates and additional information can be found on the lecture website (via EWS). The assignments will be published **Tuesdays** on a weekly basis and have to be solved until the next **Monday** unless stated otherwise. Drop your sheets into the mailbox in OH16 right across the secretariat (E22) or send an e-email to your tutor. In the latter case, the submissions must be of either **PDF** or **PS** format. To pass the labs, a minimum of 50% of the total points must be achieved.