Discrete Event Models

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Models of computation considered in this course

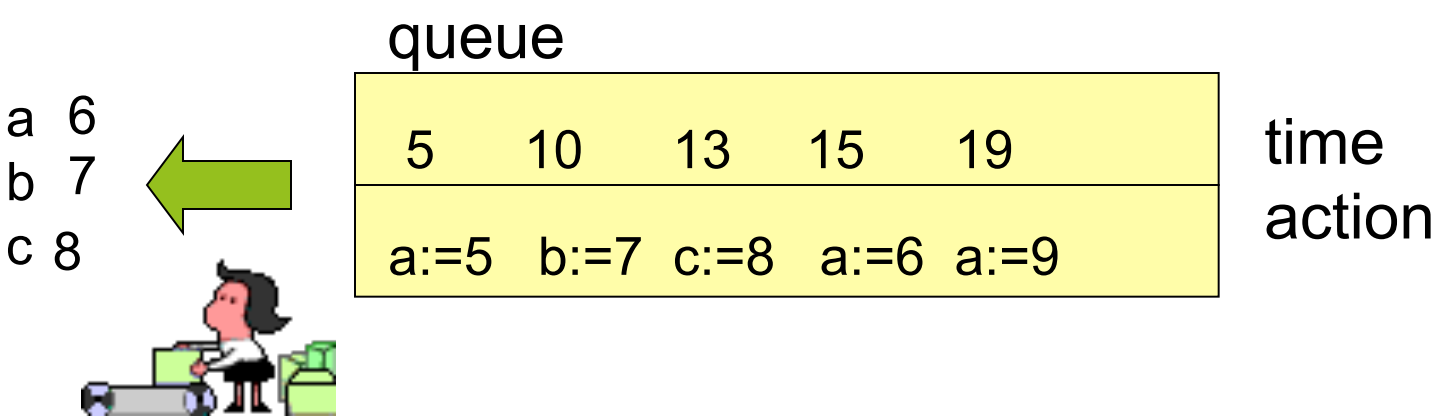
Communication/ local computations	Shared memory	Message passing Synchronous | Asynchronous
Undefined components	Plain text, use cases | (Message) sequence charts	
Communicating finite state machines	StateCharts	SDL
Data flow	Scoreboarding + Tomasulo Algorithm (☞ Comp.Archict.)	Kahn networks, SDF
Petri nets		C/E nets, P/T nets, …
Discrete event (DE) model	VHDL*, Verilog*, SystemC*, …	Only experimental systems, e.g. distributed DE in Ptolemy
Von Neumann model	C, C++, Java	C, C++, Java with libraries CSP, ADA |

* Classification is based on implementation of VHDL, Verilog, SystemC with central queue

Discrete event semantics

Basic discrete event (DE) semantics

- Queue of future actions, sorted by time
- Loop:
  - Fetch next entry from queue
  - Perform function as listed in entry
    - May include generation of new entries
- Until termination criterion = true



HDLs using discrete event (DE) semantics

Used in hardware description languages (HDLs):

Description of concurrency is a must for HW description languages!

- Many HW components are operating concurrently
- Typically mapped to “processes“
- These processes communicate via “signals“
- Examples:
  - MIMOLA [Zimmermann/Marwedel], ~1975 …
  - ….
  - VHDL (very prominent example in DE modeling)
    One of the 3 most important HDLs:
    VHDL, Verilog, SystemC

VHDL

VHDL = VHSIC hardware description language

VHSIC = very high speed integrated circuit

1980: Def. started by US Dept. of Defense (DoD) in 1980

1984: first version of the language defined, based on ADA (which in turn is based on PASCAL)

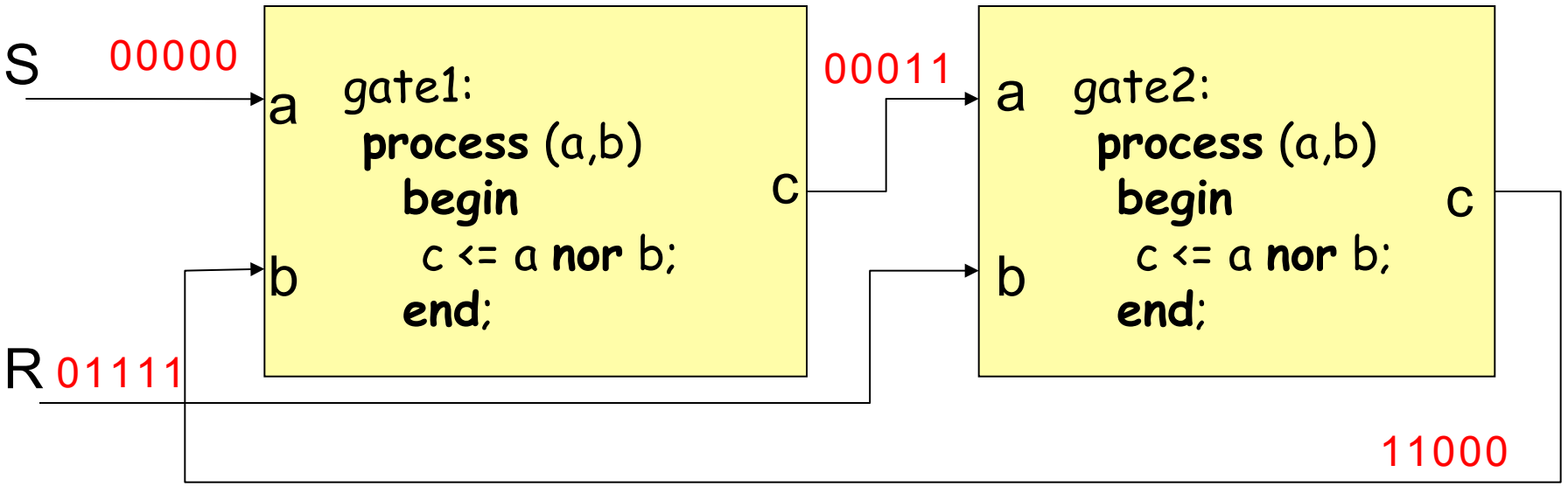
1987: revised version became IEEE standard 1076

1992: revised IEEE standard

1999: VHDL-AMS: includes analog modeling

2006: Major extensions

Simple example (VHDL notation)



Processes will wait for changes on their input ports.

If they arrive, processes will wake up, compute their code and deposit changes of output signals in the event queue and wait for the next event.

If all processes wait, the next entry will be taken from the event queue.

VHDL processes

Delays allowed:

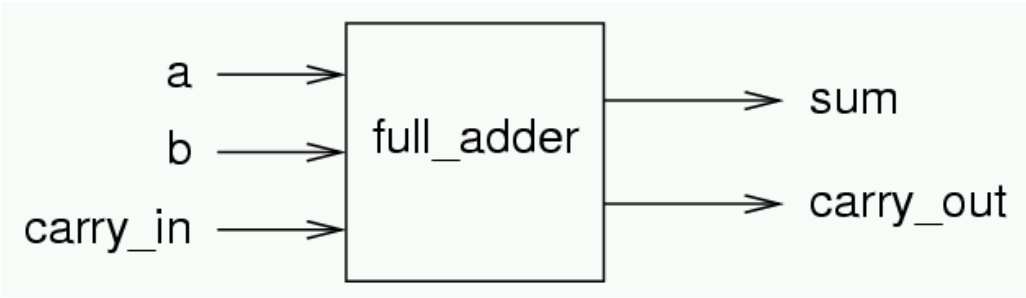
```
process (a,b)
 begin
   c <= a nor b after 10 ns;
 end;
```

Equivalent to

```
process
 begin
  c <= a nor b after 10 ns;
  wait on a,b;
 end;
```

- <=: signal assignment operator
- Each executed signal assignment will result in **adding** entries in the projected waveform, as indicated by the (optional) delay time
- Implicit loop around the code in the body
- Sensitivity lists are a shorthand for a single **wait on**-statement at the end of the process body

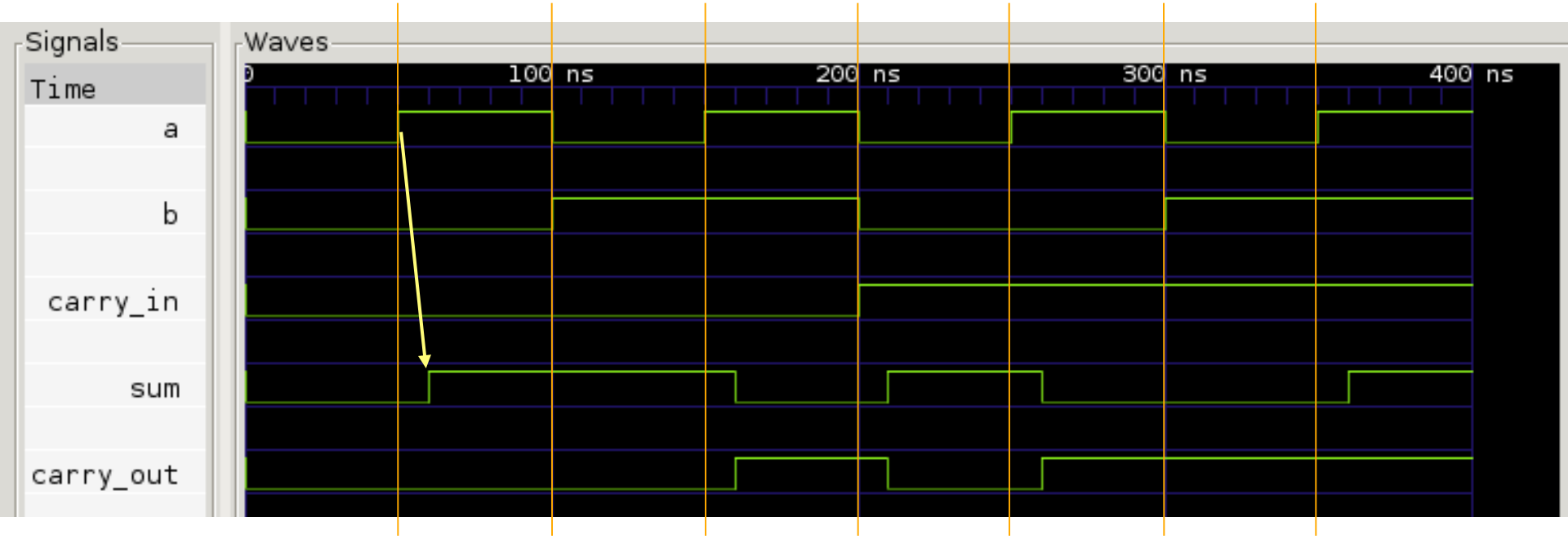
The full adder as an example




```
entity full_adder is
 port(a, b, carry_in: in Bit;  -- input ports
      sum,carry_out: out Bit); --output ports
end full_adder;

architecture behavior of full_adder is
 begin
  sum       <= (a xor b) xor carry_in after 10 ns;
  carry_out <= (a and b) or (a and carry_in) or
                (b and carry_in)       after 10 ns;
 end behavior;
```

The full adder as an example
- Simulation results -



VHDL semantics: global control

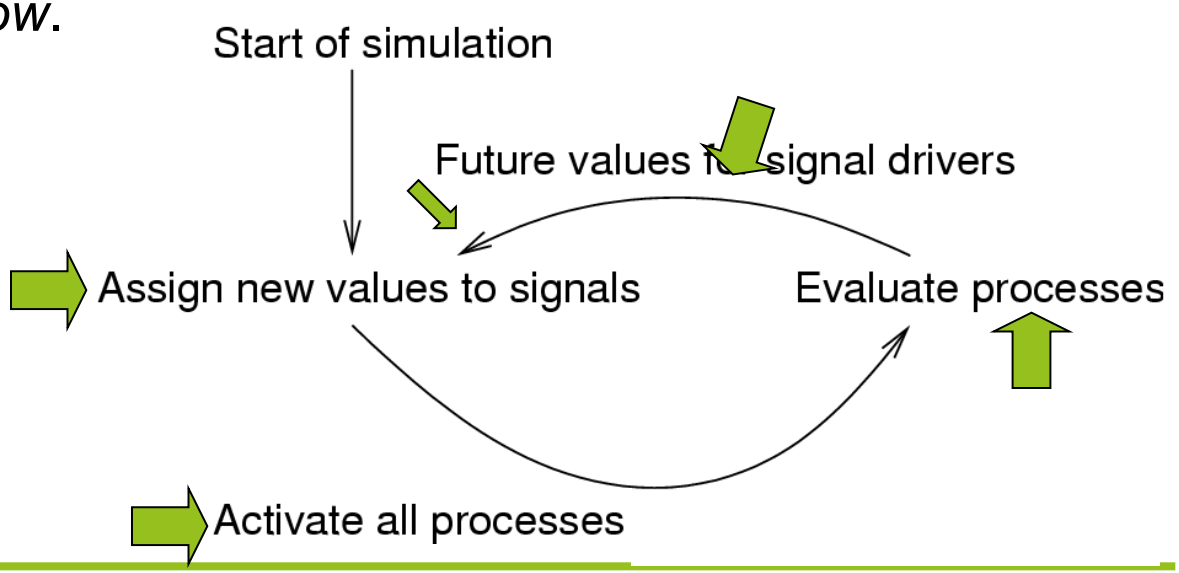
According to the original VHDL standards document:

- The execution of a model consists of an initialization phase followed by the repetitive execution of process statements in the description of that model.
- Initialization phase executes each process once.

VHDL semantics: initialization

At the beginning of initialization, the current time, T_c is 0 ns.

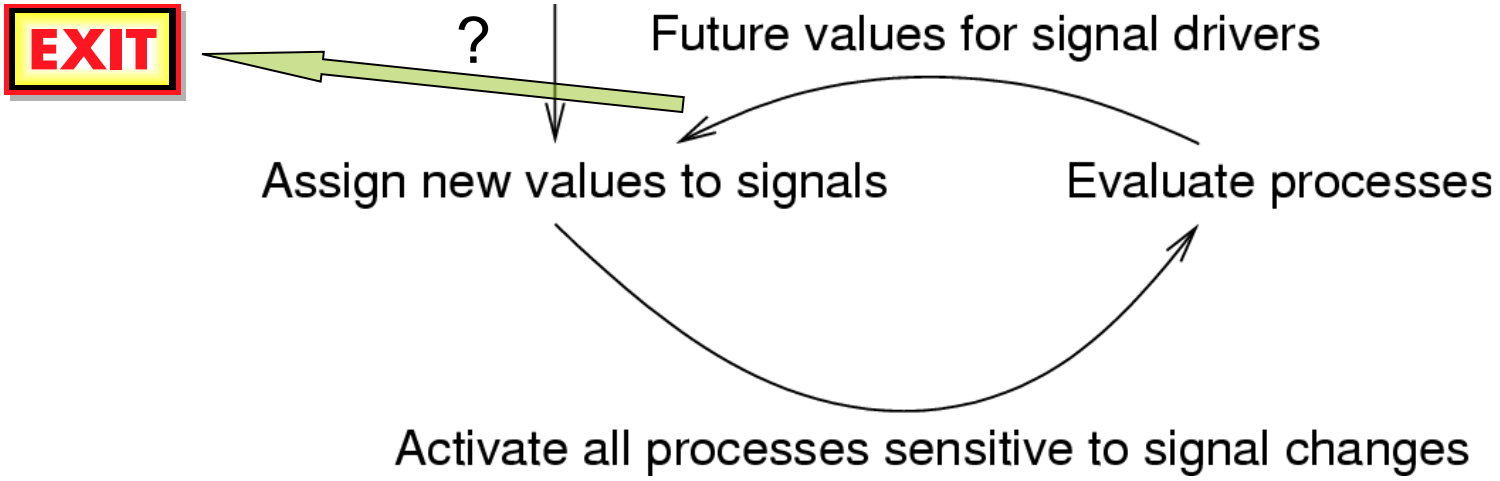
- *The … effective value of each explicitly declared signal are computed, and the current value of the signal is set to the effective value. …*
- *Each ... process … is executed until it suspends.*
- *The time of the next simulation cycle (… in this case … the 1st cycle), T_n is calculated according to the rules of step f of the simulation cycle, below.*



VHDL semantics: The simulation cycle (1)

According to the standard, the simulation cycle is as follows:

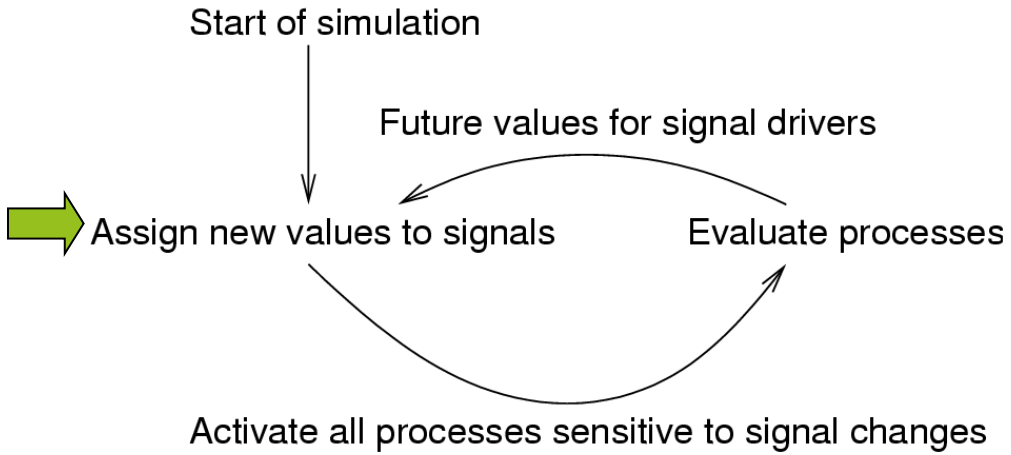
a) Stop if T_n= time'high
and "nothing else is to be done" at T_n.
The current time, T_c is set to T_n.



VHDL semantics: The simulation cycle (2)

a) ***Each active explicit signal in the model is updated. (Events may occur as a result.)***
Previously computed entries in the queue are now assigned if their time corresponds to the current time T_c.
New values of signals are not assigned before the next simulation cycle, at the earliest.
Signal value changes result in events ☞ enable the execution of processes that are sensitive to that signal.

b) ..

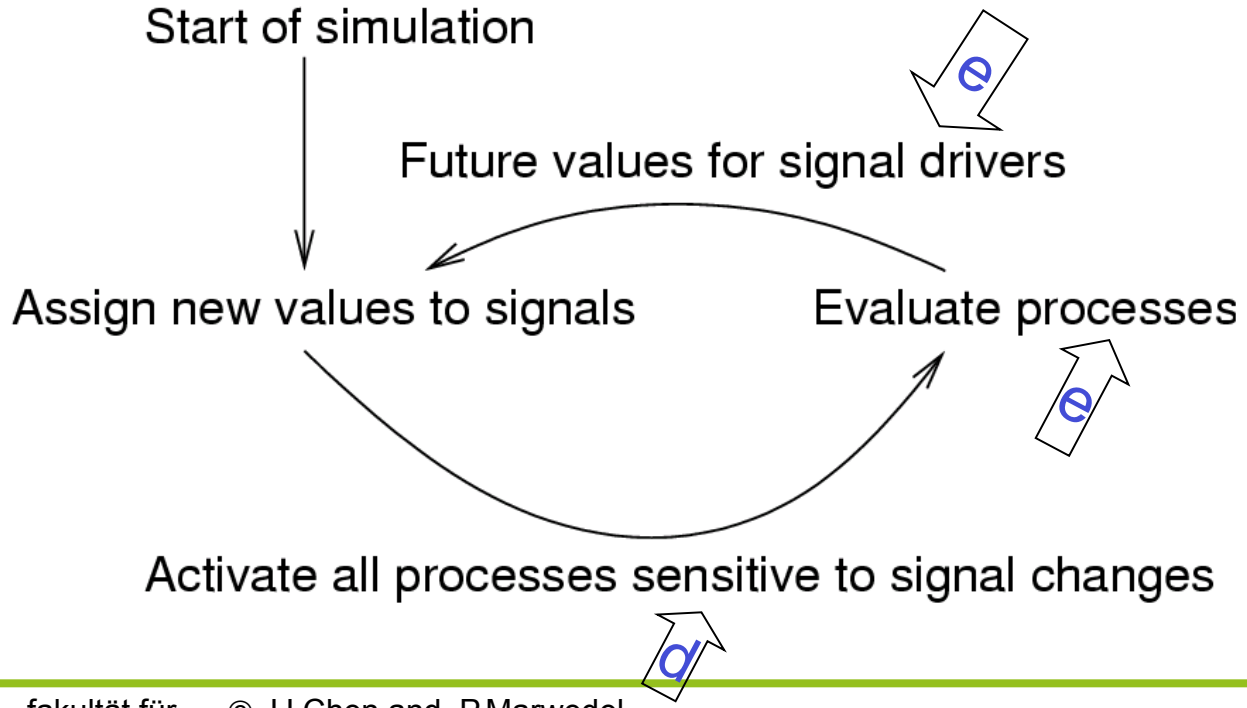


VHDL semantics: The simulation cycle (3)

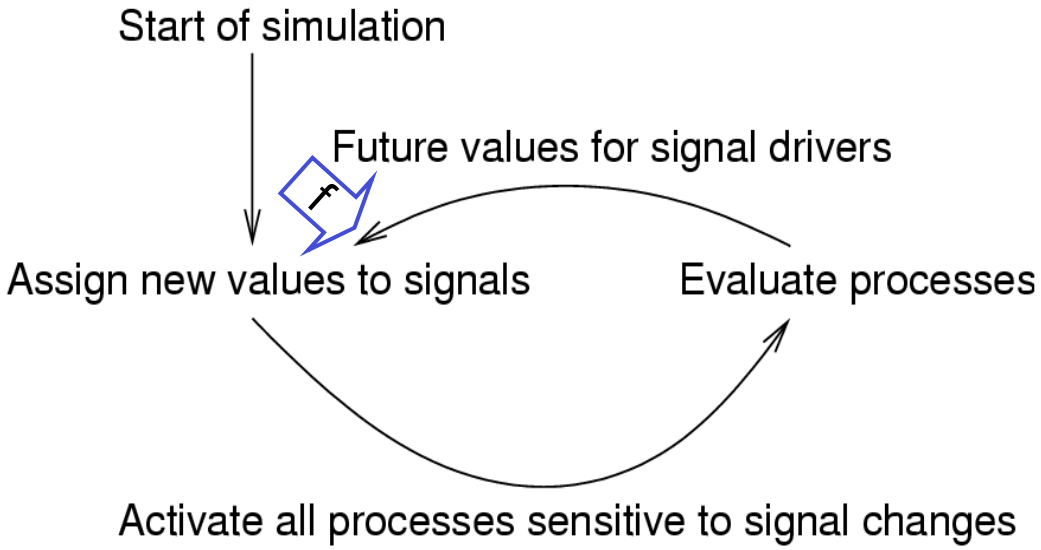
a) ∀ P sensitive to s: if event on s in current cycle: P resumes.

b) Each ... process that has resumed in the current simulation cycle is executed until it suspends*.

*Generates future values for signal drivers.



VHDL semantics: The simulation cycle (4)

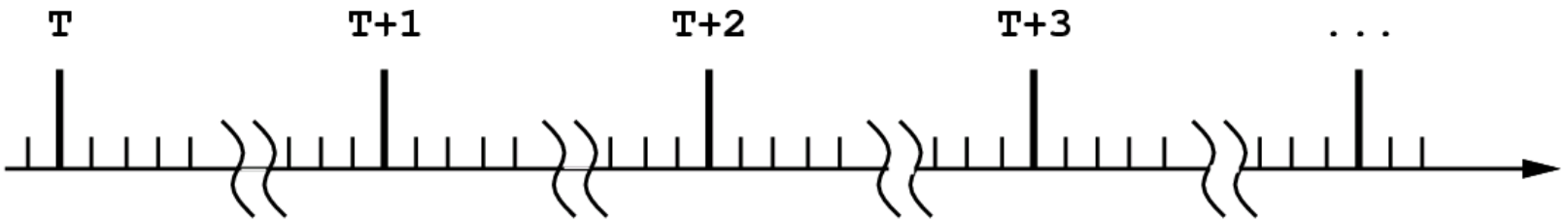


a) Time T_n of the next simulation cycle = earliest of
   1. time‘high (end of simulation time).
   2. The next time at which a driver becomes active
   3. The next time at which a process resumes (determined by **wait for** statements).

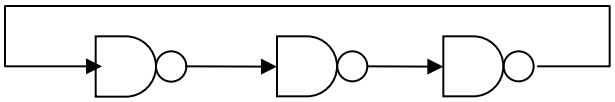
Next simulation cycle (if any) will be a delta cycle if $T_n = T_c$.

δ-simulation cycles

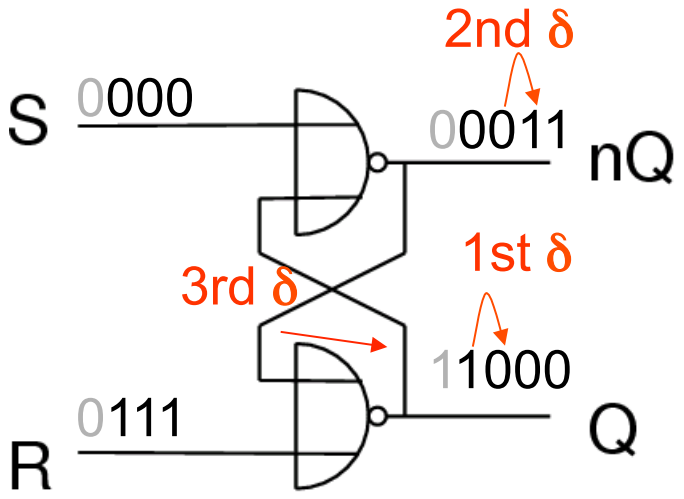
…
Next simulation cycle (if any) will be a delta cycle if $T_n = T_c$.
Delta cycles are generated for delay-less models.
There is an arbitrary number of δ cycles between any 2 physical time instants:



In fact, simulation of delay-less hardware loops might not terminate (don't even advance T_c).



δ-simulation cycles
Simulation of an RS-Flipflop




```
gate1:
   process (S,Q)
    begin
       nQ <= S nor Q;
    end;
gate2:
   process (R,nQ)
    begin
       Q <= R nor nQ;
    end;
```

	0ns	0ns+δ	0ns+2δ	0ns+3δ
R	1	1	1	1
S	0	0	0	0
Q	1	0	0	0
nQ	0	0	1	1

δ cycles reflect the fact that no real gate comes with zero delay.

☞ should delay-less signal assignments be allowed at all?

δ-simulation cycles and determinate simulation semantics

Semantics of

a <= b;

b <= a; ?

Separation into 2 simulation phases results in determinate semantics (☞ StateMate).