technische universität dortmund

Bachelor/Master Thesis

FPGA-based Memory Access Analysis for Non-Volatile Main Memory

Kuan-Hsun Chen
Prof. Dr. Jian-Jia Chen
Otto-Hahn-Str. 16
Technische Universität Dortmund
Email: kuan-hsun.chen@tu-dortmund.de
17.06.2019

Emerging non-volatile memory (NVM) technologies, such as Phase Change Memory, have been considered to serve as main memory due to the features of low leakage power, high density, and low unit costs. However, such NVMs face a significantly lower write endurance compared to the classic DRAM. Since this would lead to premature system failures during normal software execution, several approaches propose to distribute the memory accesses of running applications evenly over the memory to feature the maximum memory lifetime. valuate these approaches, cycle accurate system simulations (e.g., gem5 and NVMain) can capture the resulting memory access behavior, but require very long simulation times usually.

Figure 1: Ultra96-V2 Development Board features a ARM® Cortex-A53 platform together with a Programable Logic

Alternatively, we would like to develop a simulation hardware, which uses an FPGA to count the memory accesses like Trace Monitoring System [1] uses an FPGA board plugged in a DIMM slot. For architectures like the Xilinx UltraScale+, FPGA can be accessed through large memory regions in the logical address space. Thus, the CPU can use these memory regions as the program's DRAM, resulting in every memory access being redirected to the FPGA. By implementing an appropriate FPGA design, we can capture the memory access behavior and store aggregated results (e.g. write counts to memory regions) directly inside the DRAM.

In this thesis, students first will study the Vivado Suite to design the FPGA circuits and process main memory requests on the FPGA. At least, real DRAM content has to be provided as the result of the memory request and a counter for the accessed memory region has to be increased. Students should configure and connect two central components, the DMA and the axi_mm2s_mapper to access the DRAM from the FPGA to return results and map memory requests from the CPU to the FPGA, respectively. At the end, the simulation hardware should be evaluated by reasonable experiments, e.g., using the state-of-the-art wear-leveling techniques to demonstrate the results. Please note that, the involved source code this thesis will be publicly released and should be fully documented to practice the rationale of open-source software development.

Other suggestions and related topics are also welcome. Please do not hesitate to make an appointment.

Required Skills:

- Knowledgeable of FPGA programming
- Comfortable with system programming in Linux
- Computer architecture knowledge is required

Acquired Skills after the thesis:

- Knowledge of FPGA
- Knowledge of non-volatile main memory
- Knowledge about modern memory bus architectures

[1] Y Bao et al., HMTT: A Platform Independent Full-System Memory Trace Monitoring System, https://dl.acm.org/citation.cfm?id=1375484